

FIG. 1

USAGE

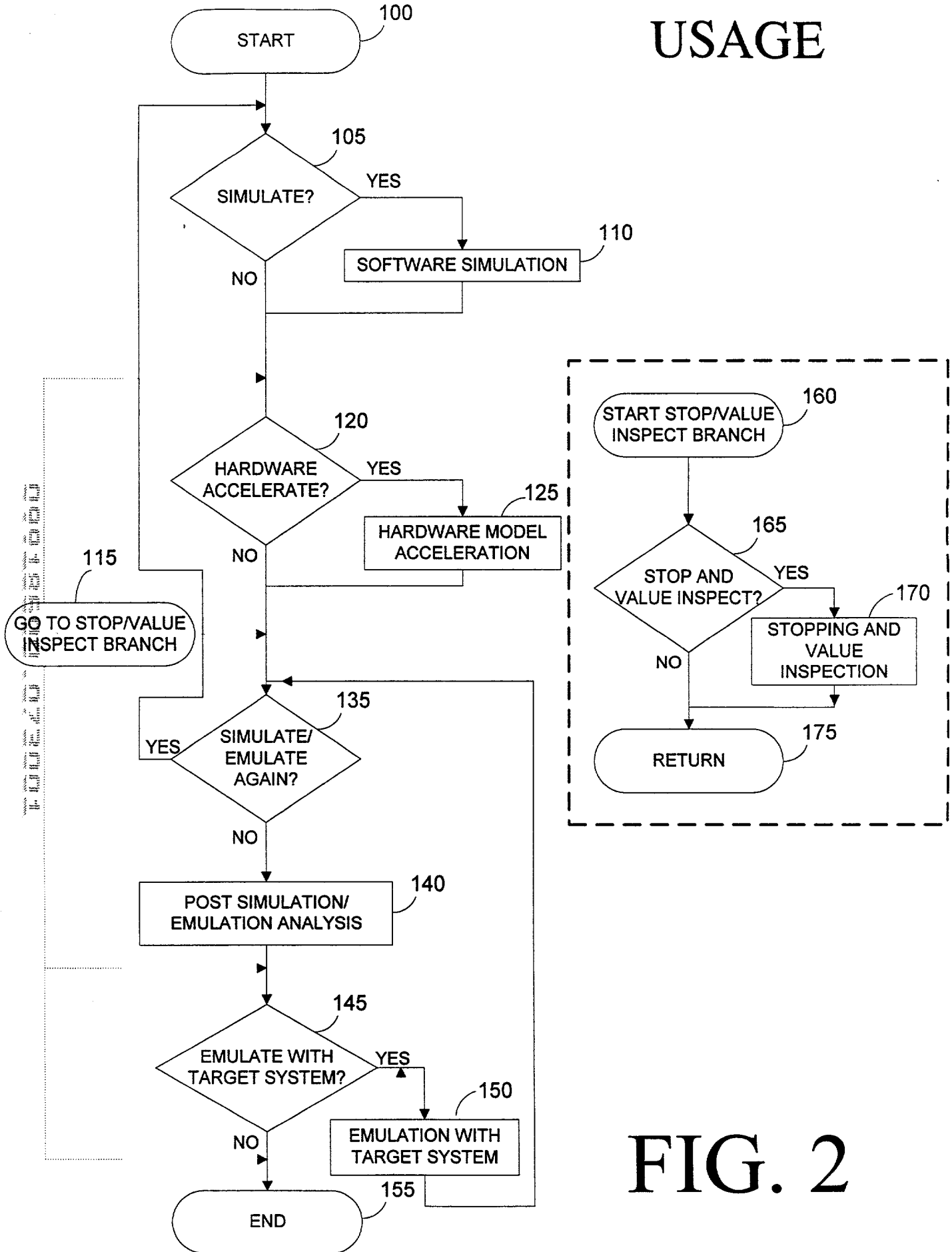


FIG. 2

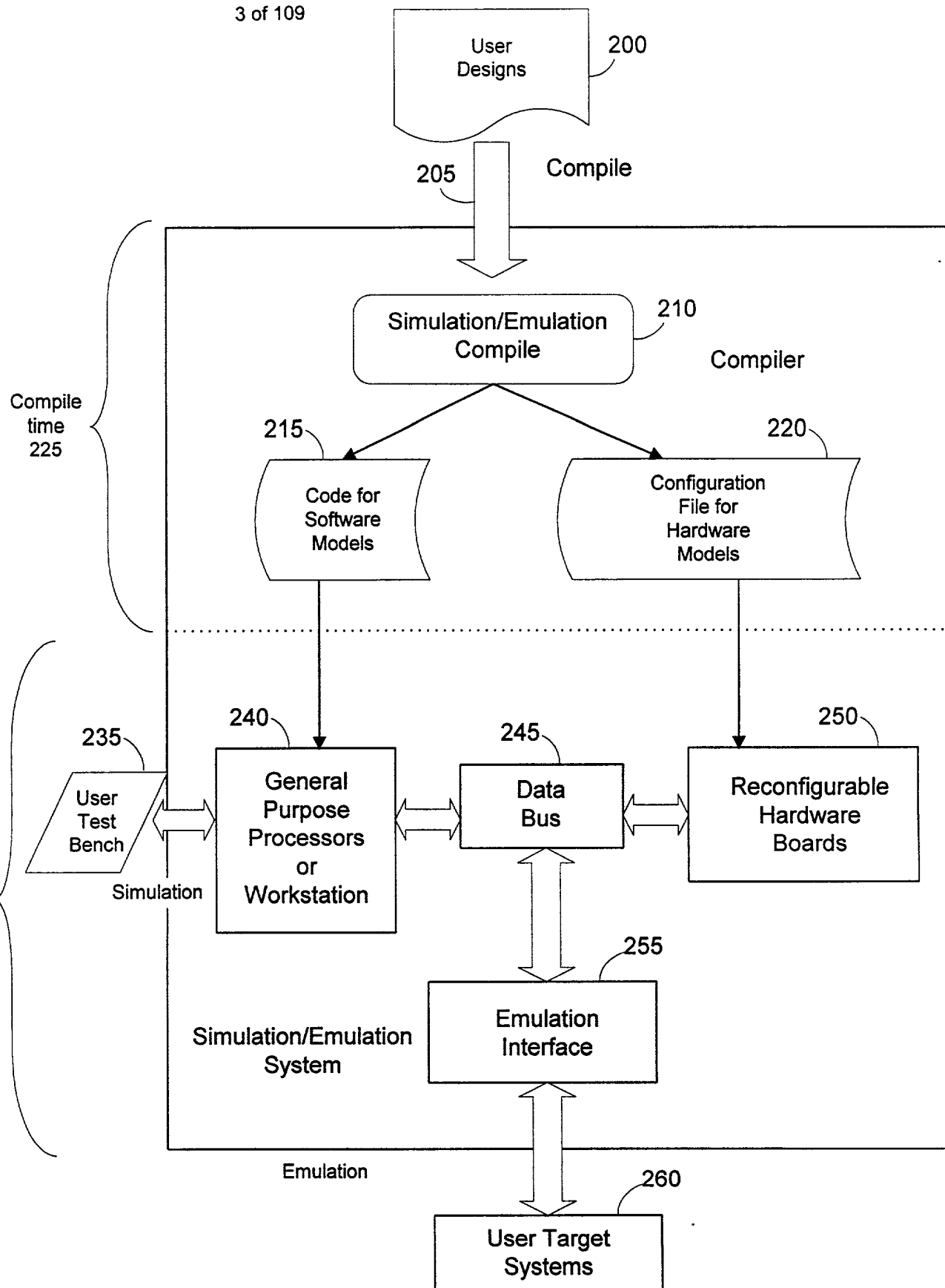


FIG. 3

COMPILATION

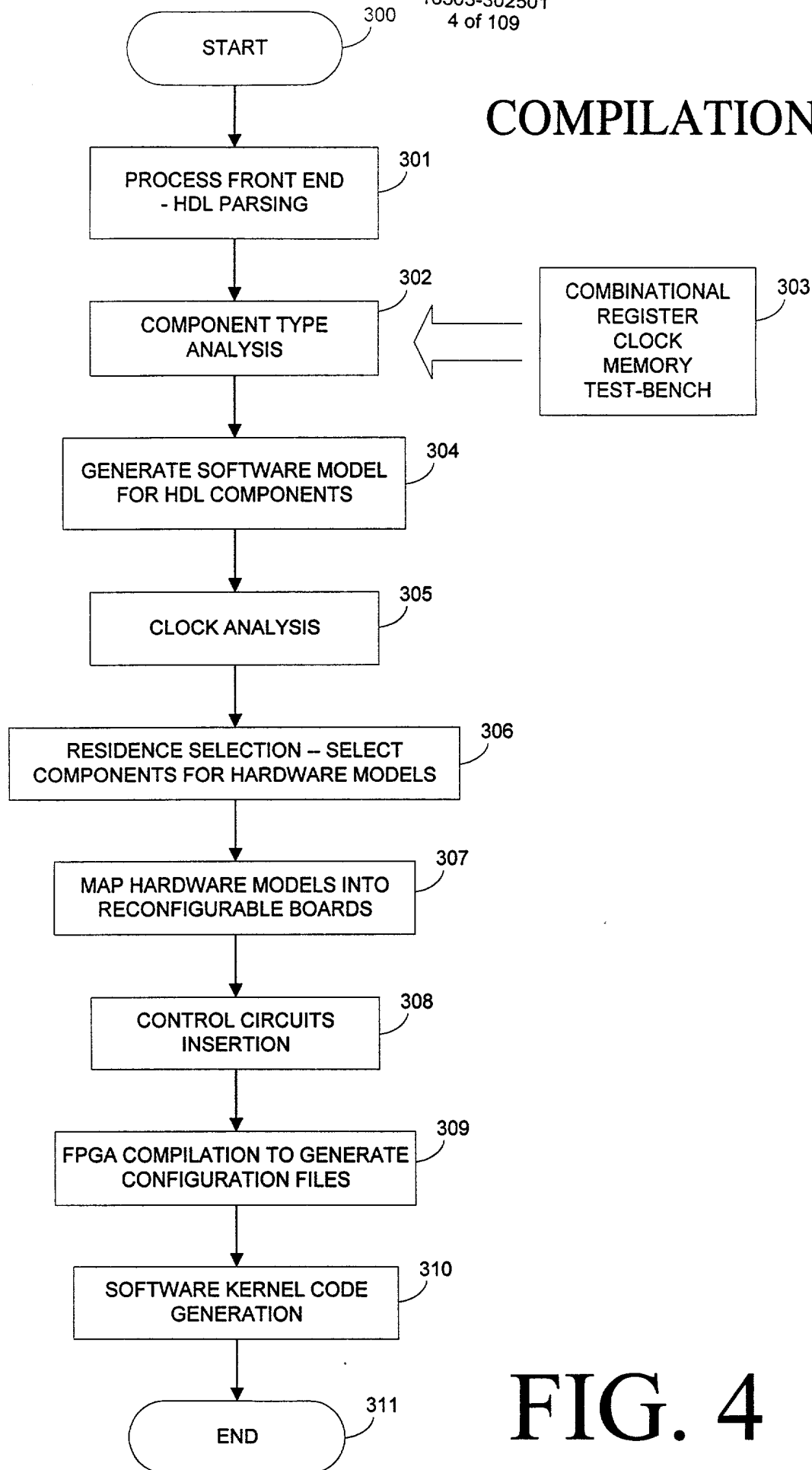


FIG. 4

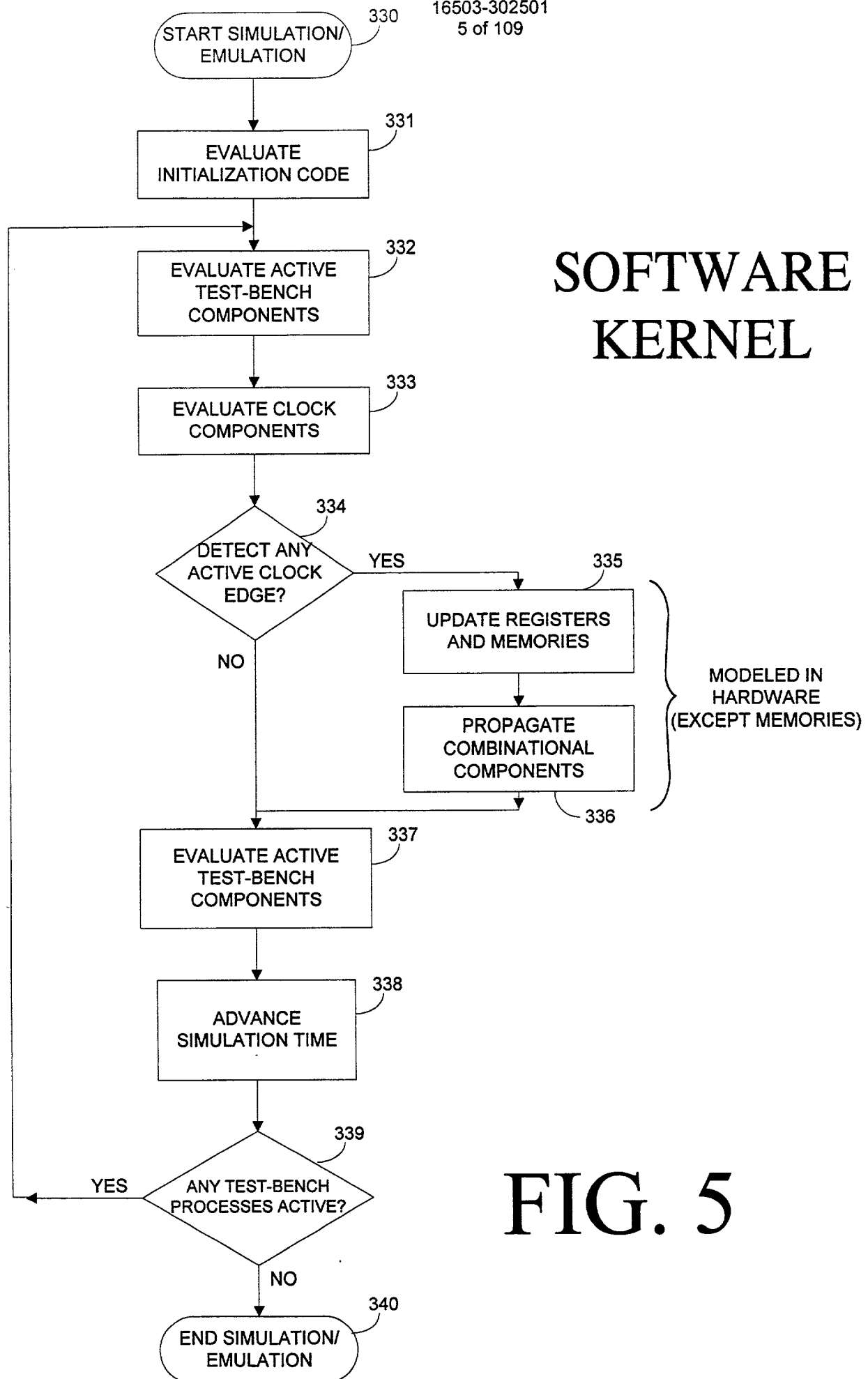


FIG. 5

MAPPING HARDWARE MODELS TO RECONFIGURABLE BOARDS

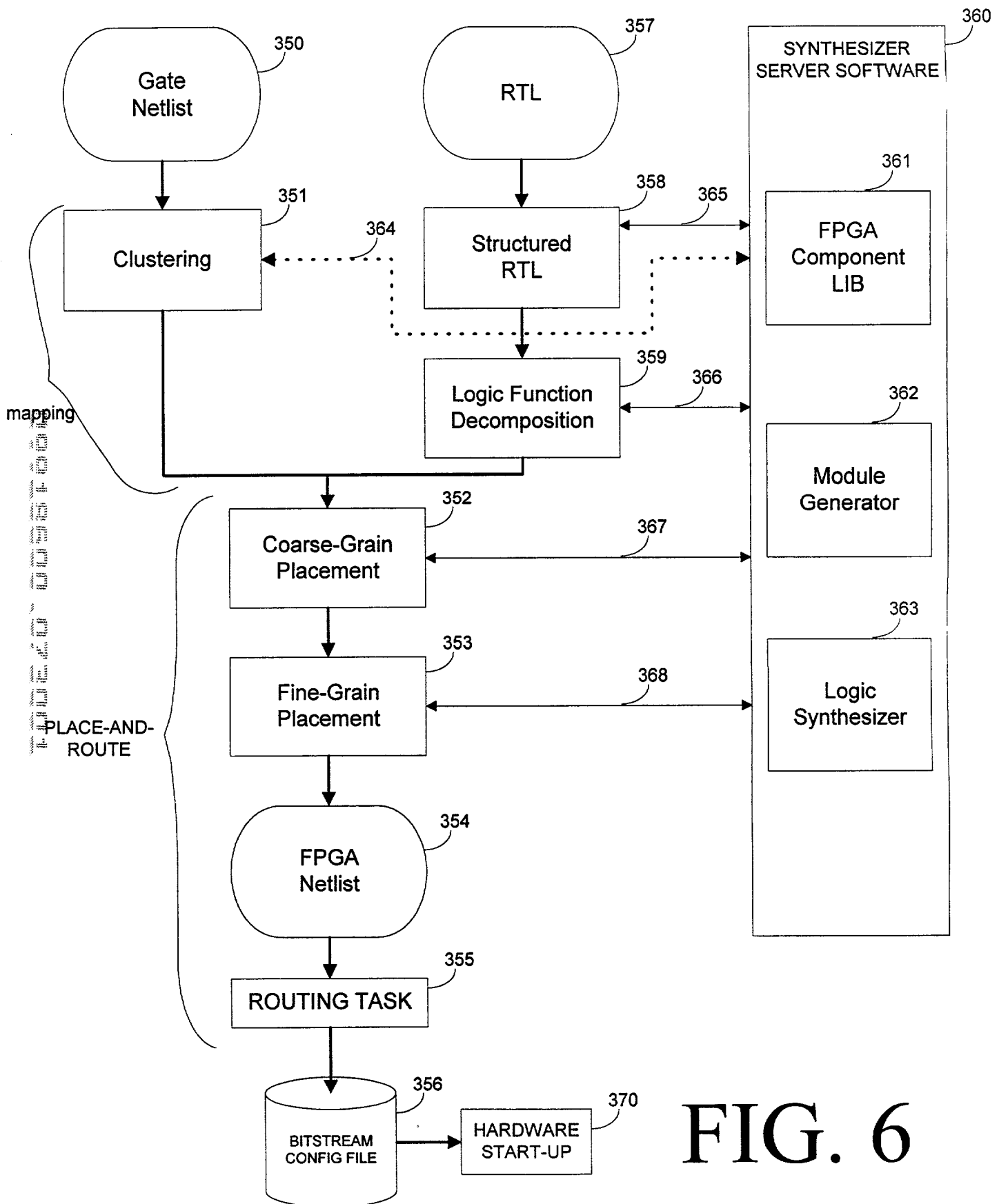


FIG. 6

	F11	F12	F13	F14	F21	F22	F23	F24	F31	F32	F33	F34	F41	F42	F43	F44
F11	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0
F12	1	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0
F13	1	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0
F14	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1
F21	0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0
F22	1	1	0	0	1	1	1	1	0	1	0	0	0	1	0	0
F23	0	0	1	0	1	1	1	1	0	0	1	0	0	0	1	0
F24	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0	1
F31	0	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0
F32	1	1	0	0	0	1	0	0	1	1	1	1	0	1	0	0
F33	0	0	1	0	0	0	1	0	1	1	1	1	0	0	1	0
F34	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0	1
F41	0	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1
F42	1	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1
F43	0	0	1	0	0	0	1	0	0	0	1	0	1	1	1	1
F44	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	1

FIG. 7

FPGA INTERCONNECTION

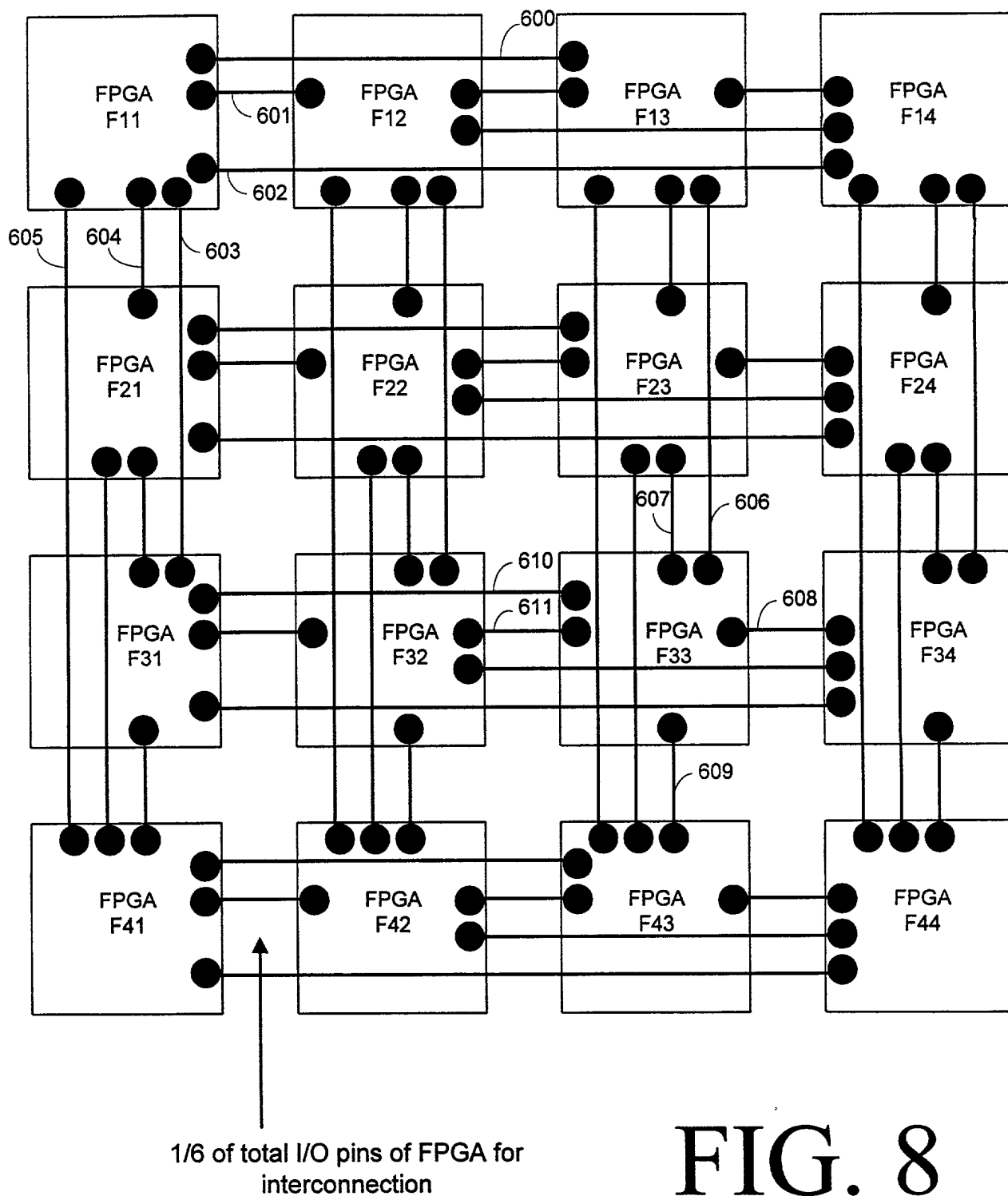


FIG. 8

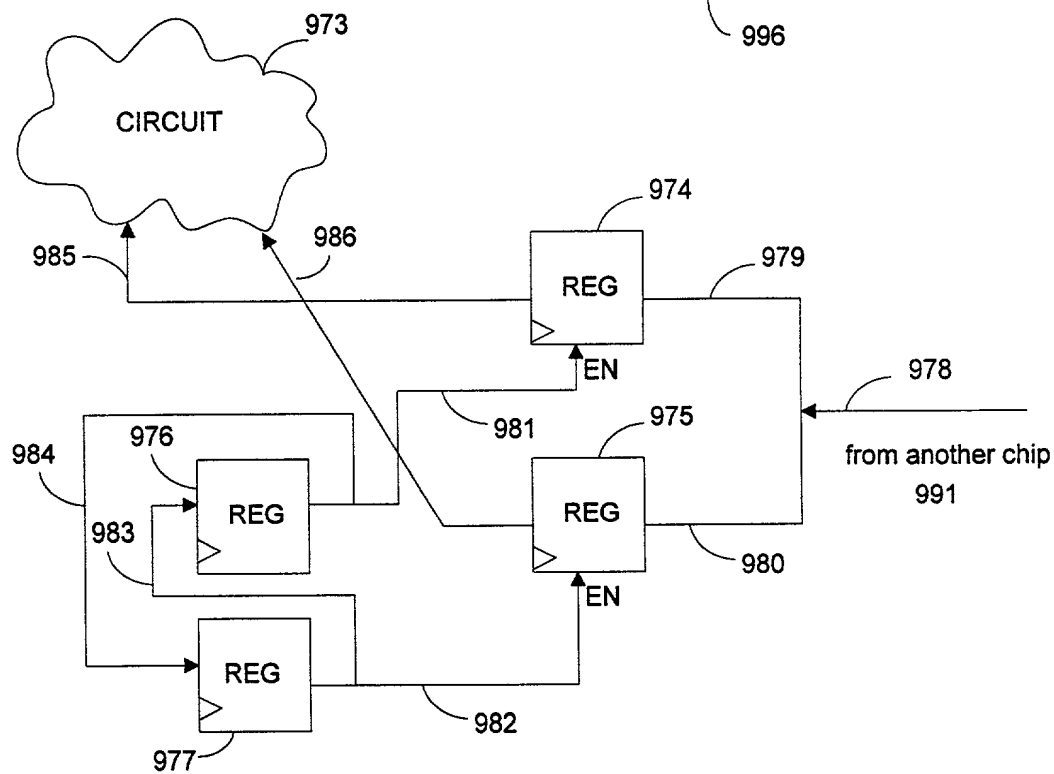
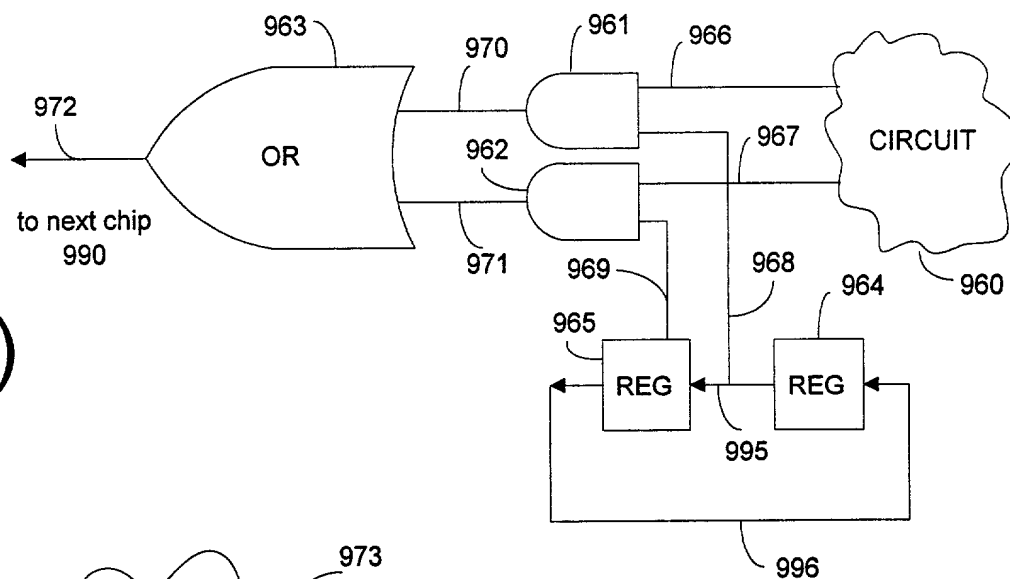
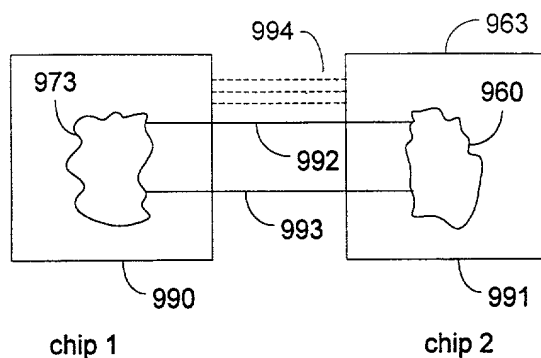


FIG. 9

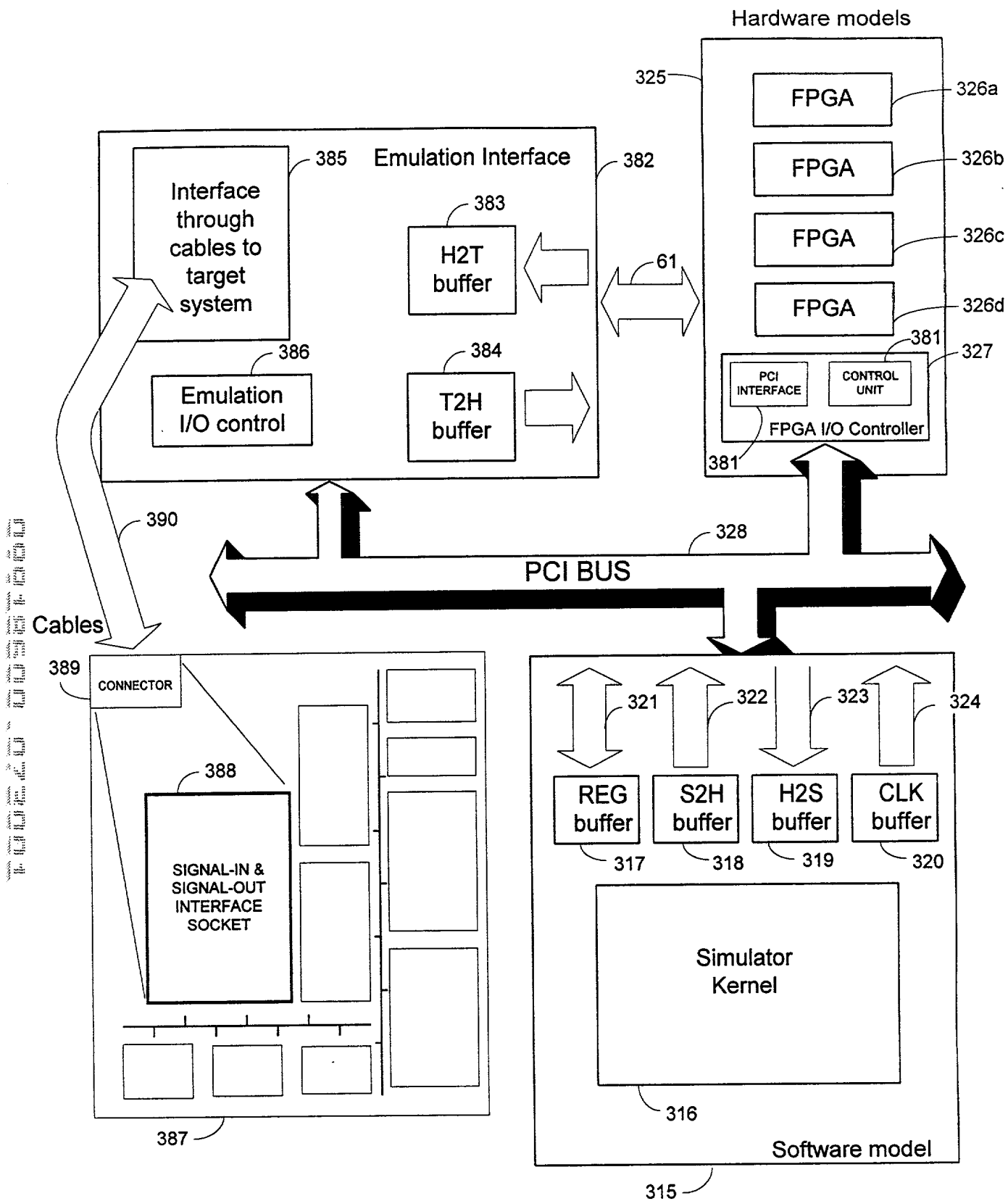


FIG. 10

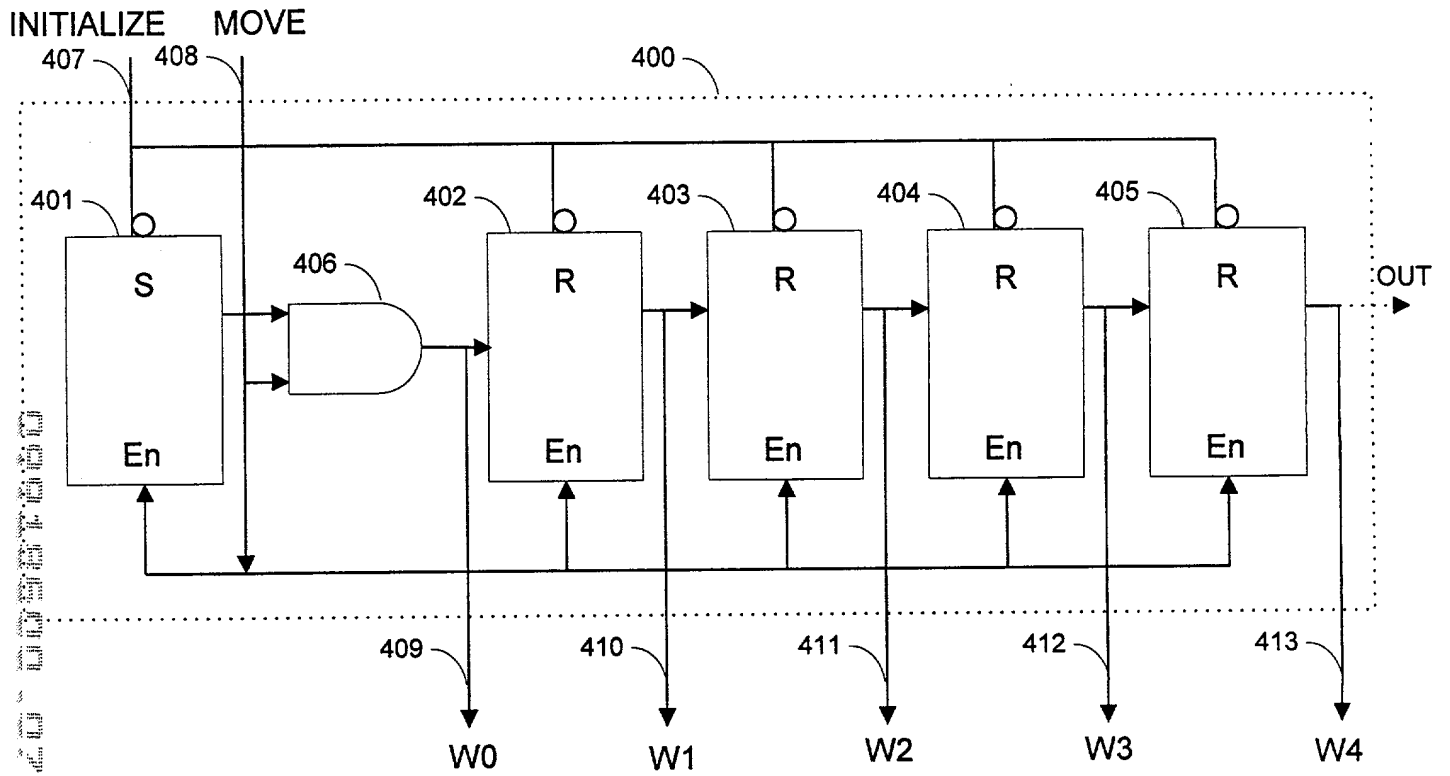


FIG. 11

ADDRESS POINTER INITIALIZATION

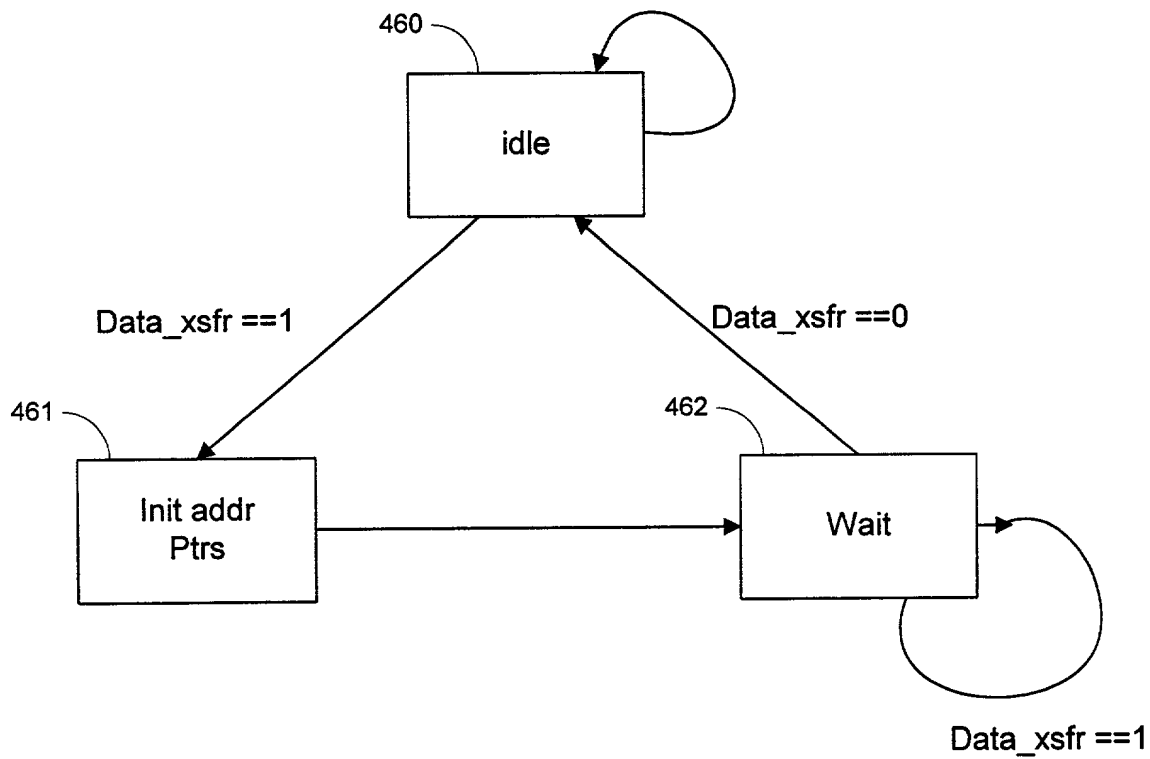


FIG. 12

EACH SEM-FPGA CHIP

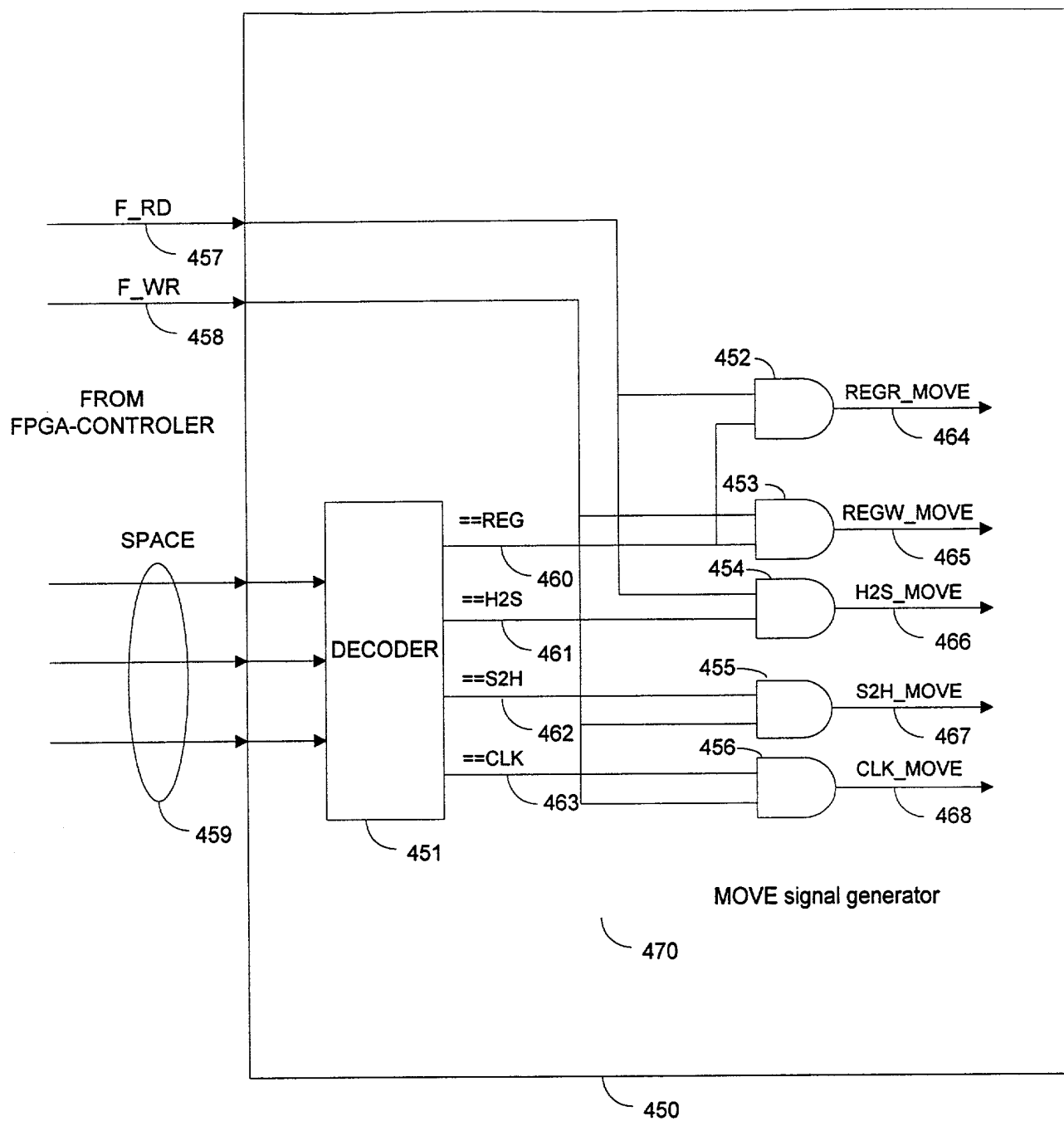


FIG. 13

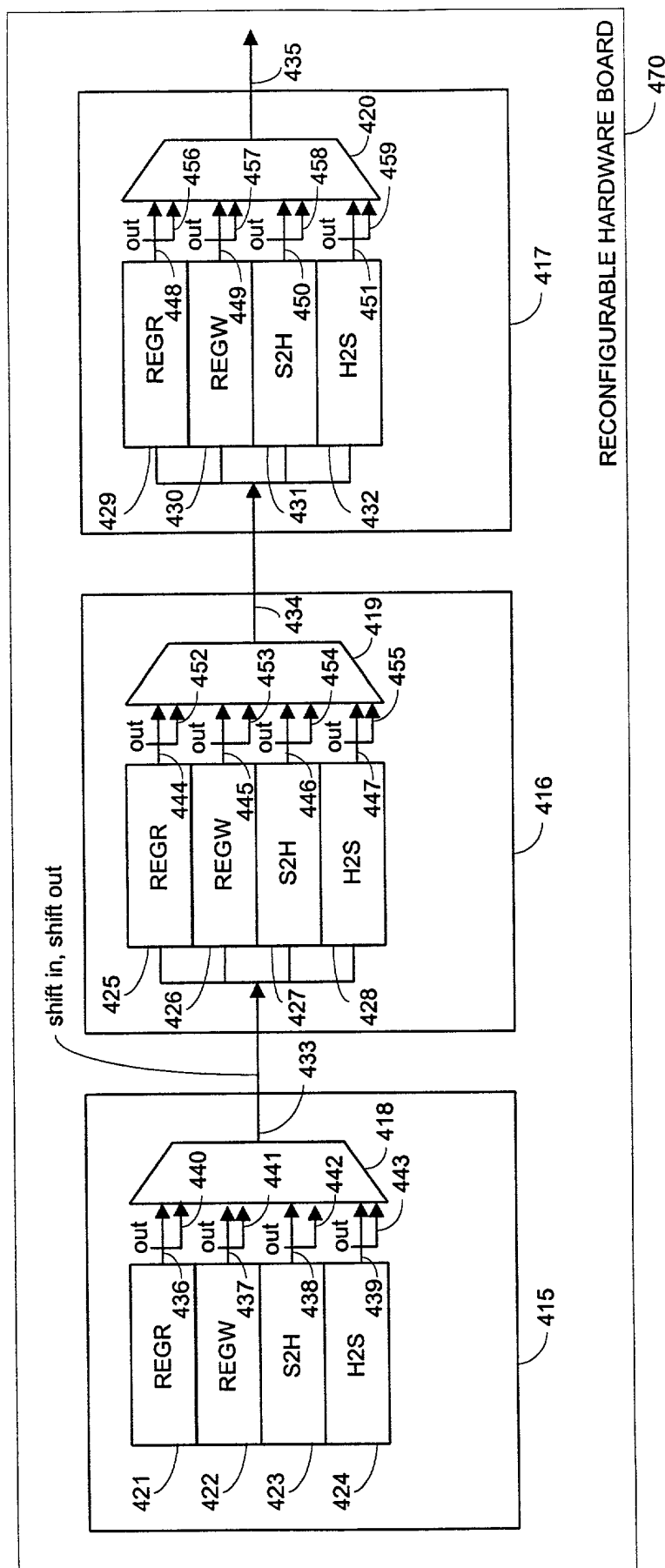


FIG. 14

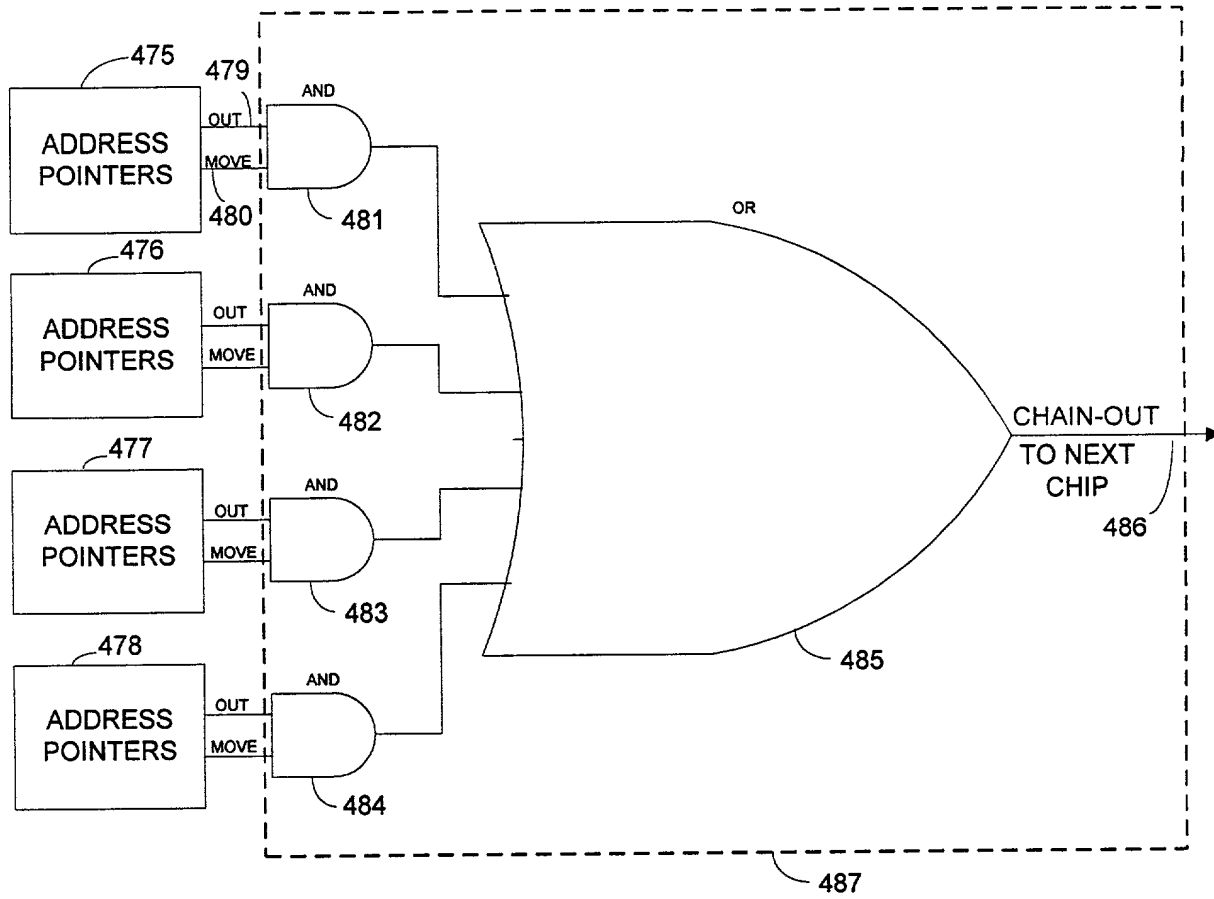


FIG. 15

GATED DATA/CLOCK ANALYSIS

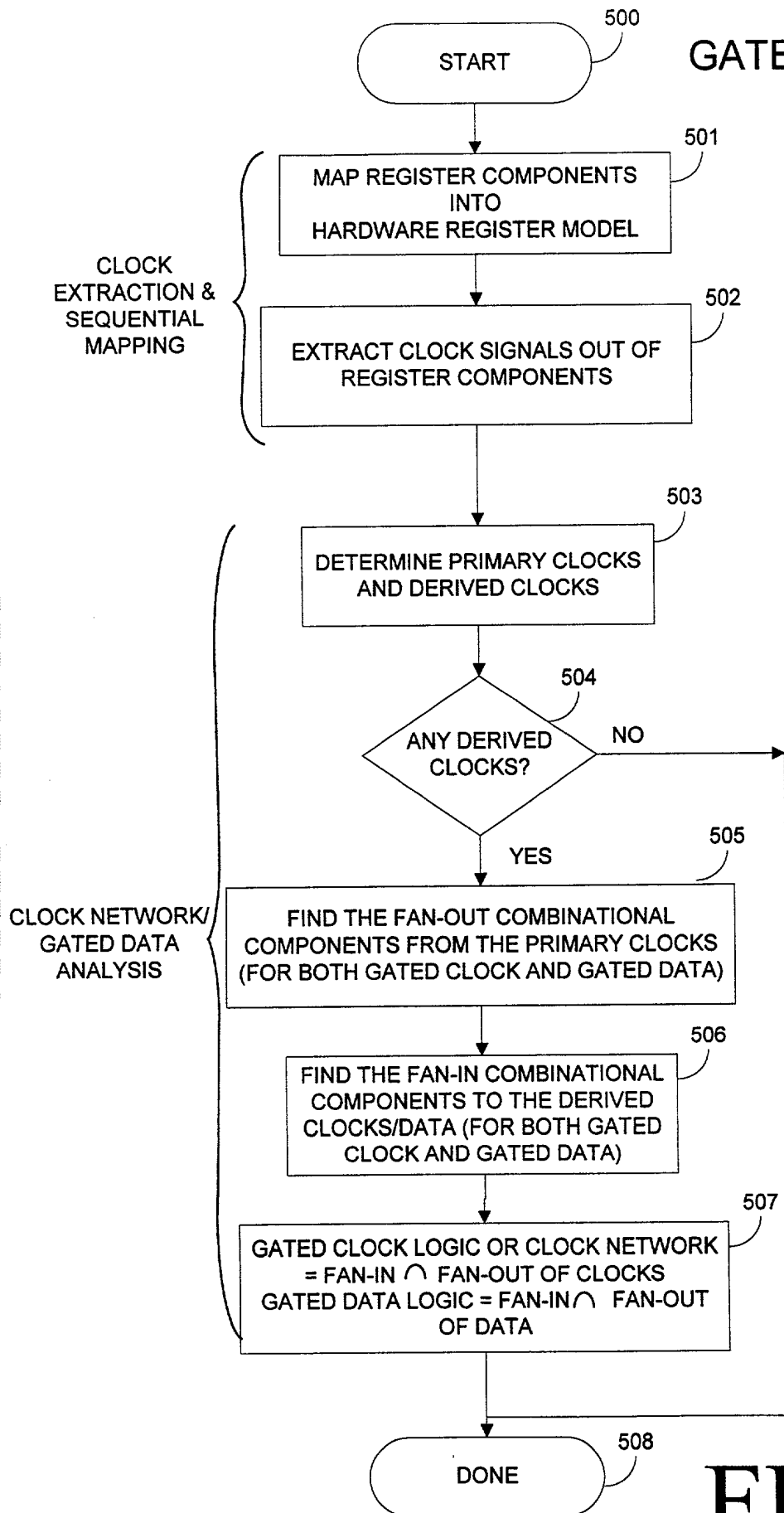


FIG. 16

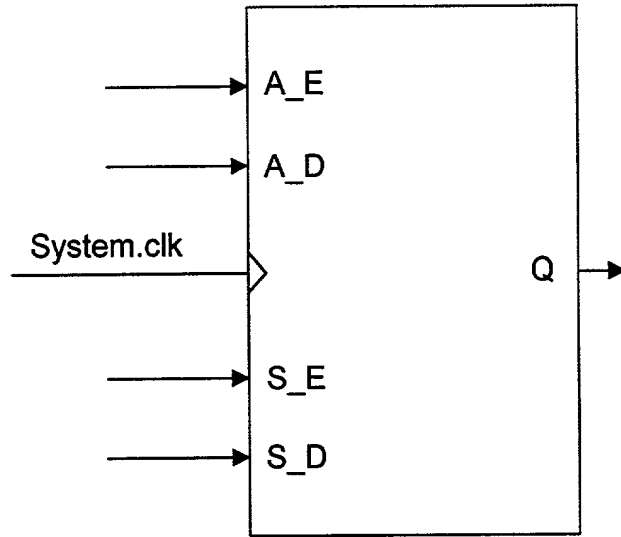


FIG. 17

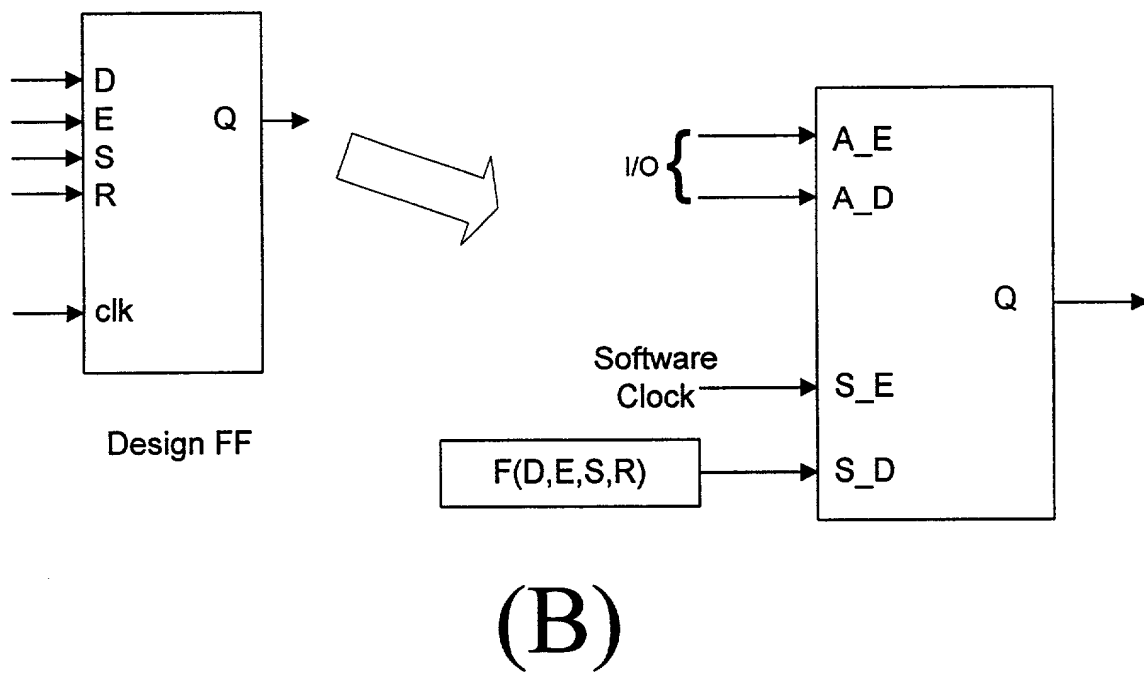
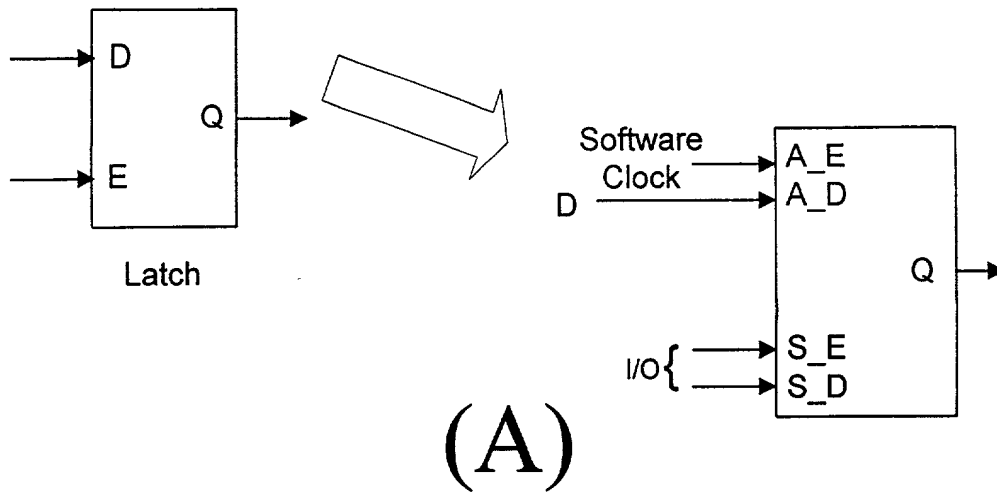


FIG. 18

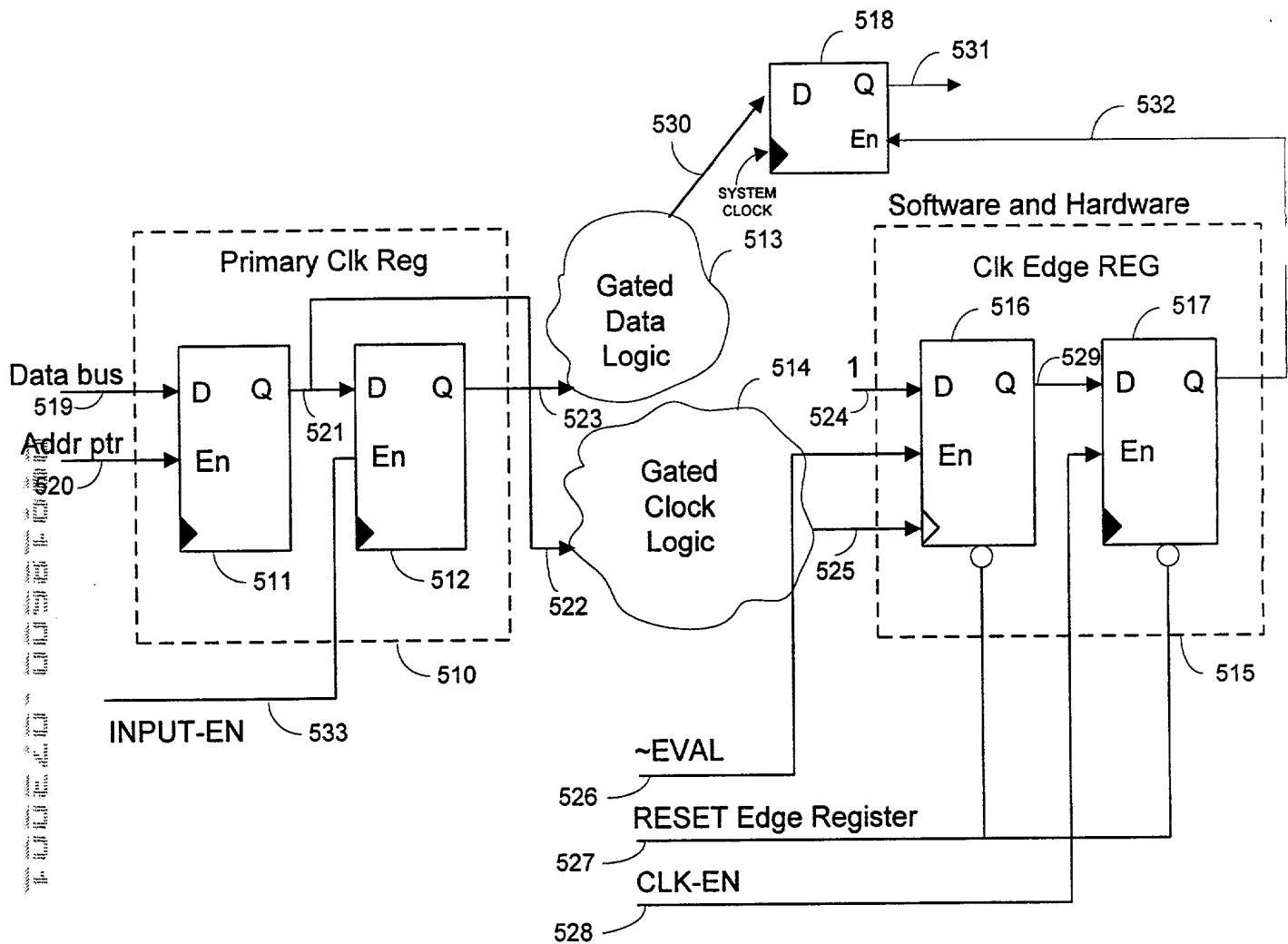


FIG. 19

DURING EVALUATION

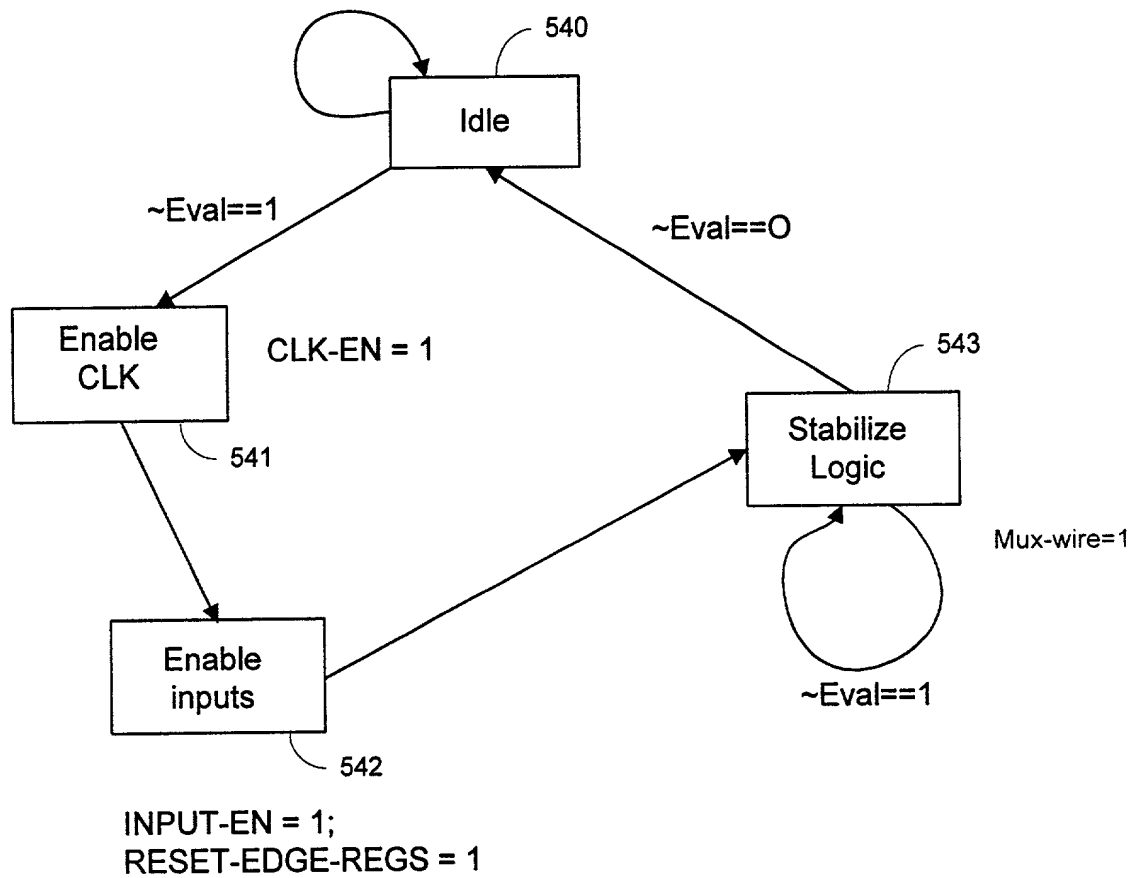


FIG. 20

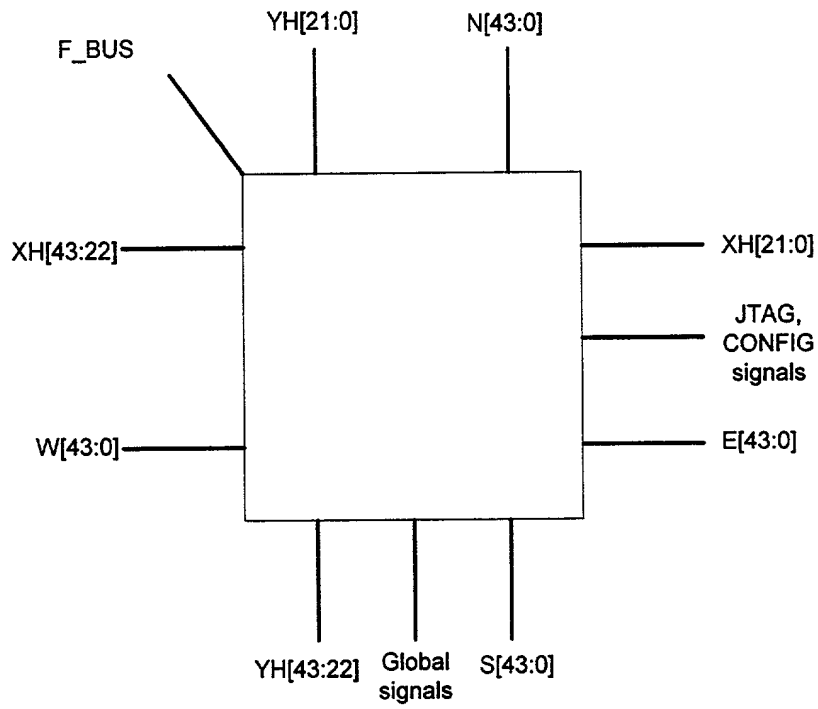


FIG. 21



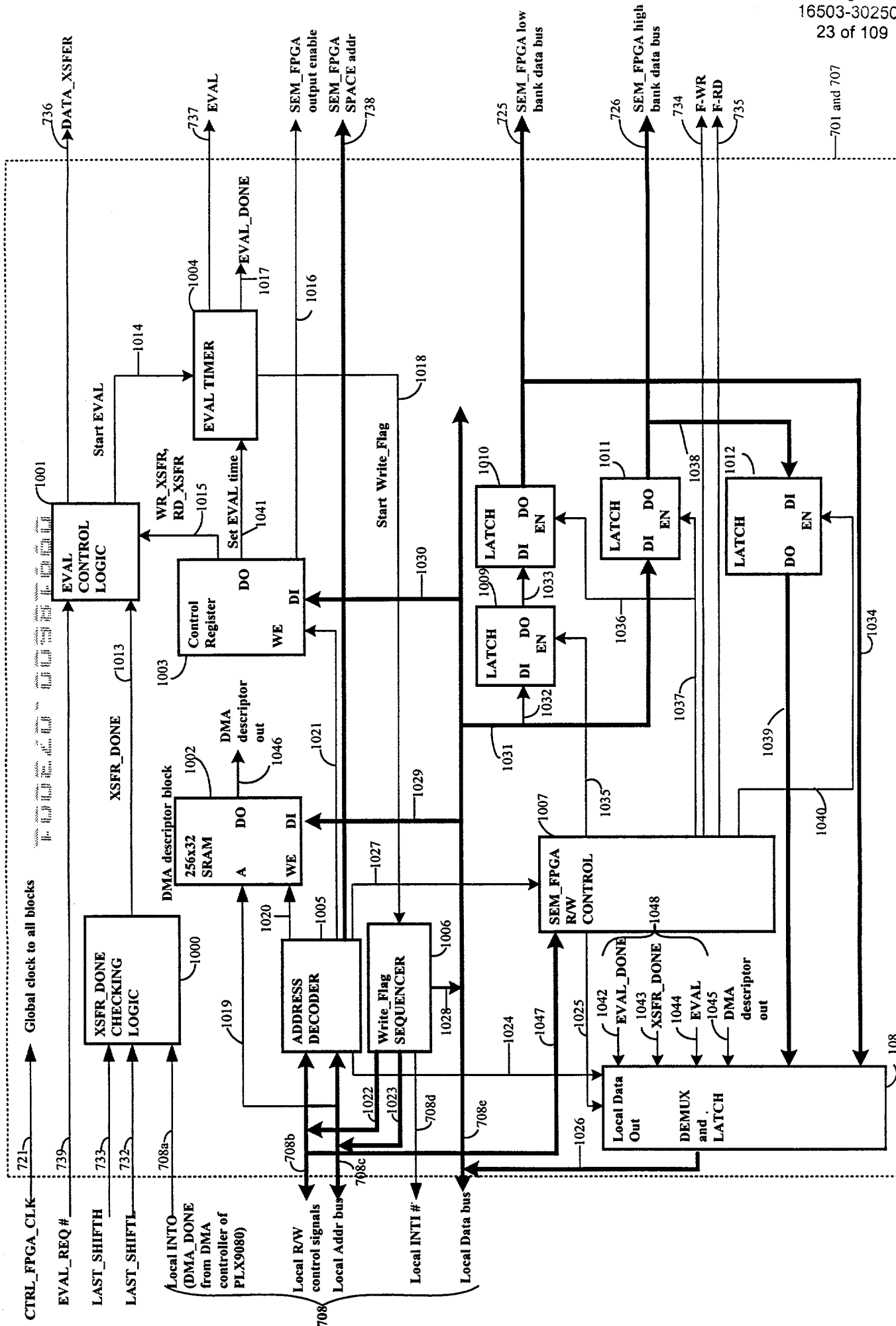


FIG. 23

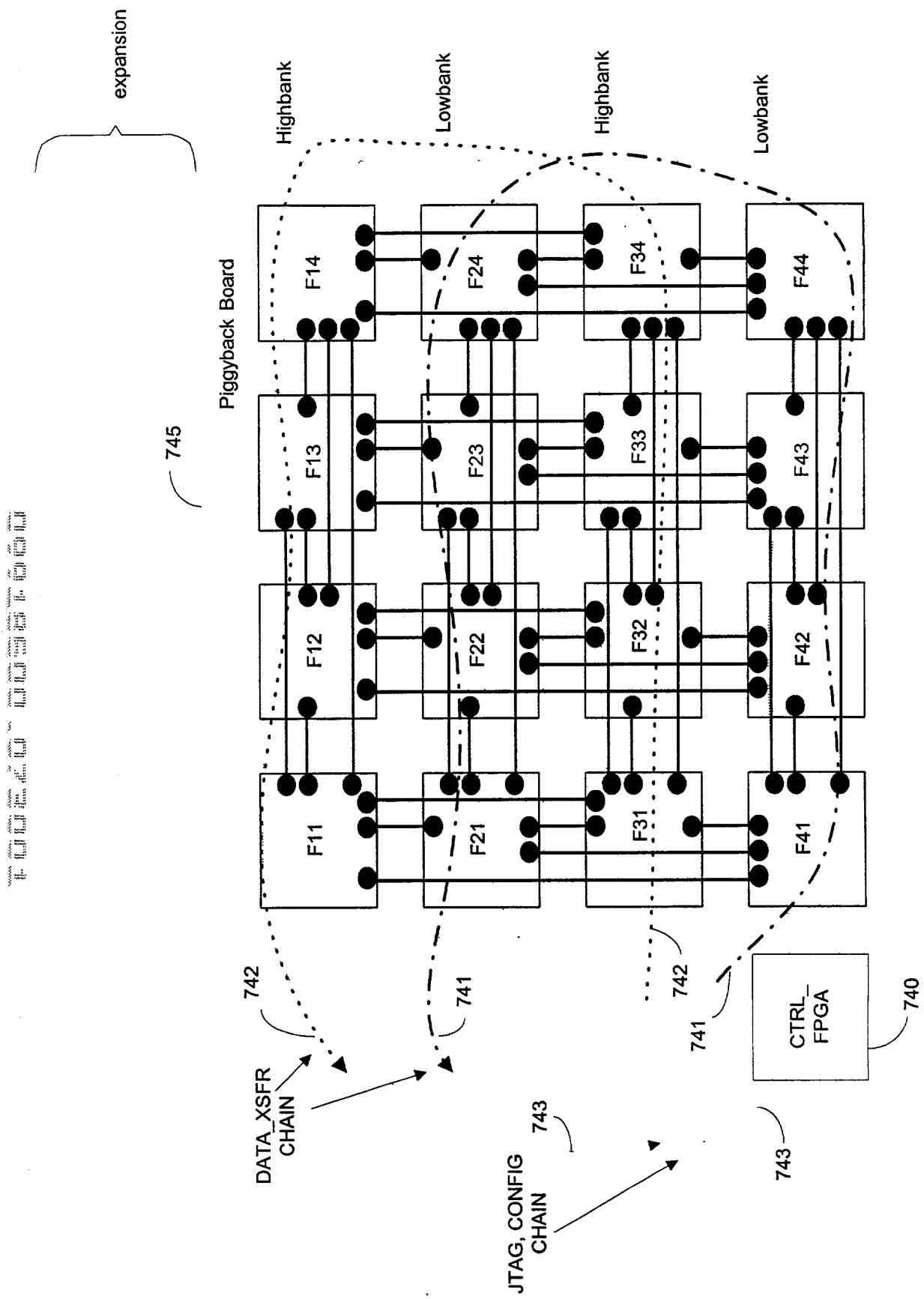


FIG. 24

HARDWARE START-UP

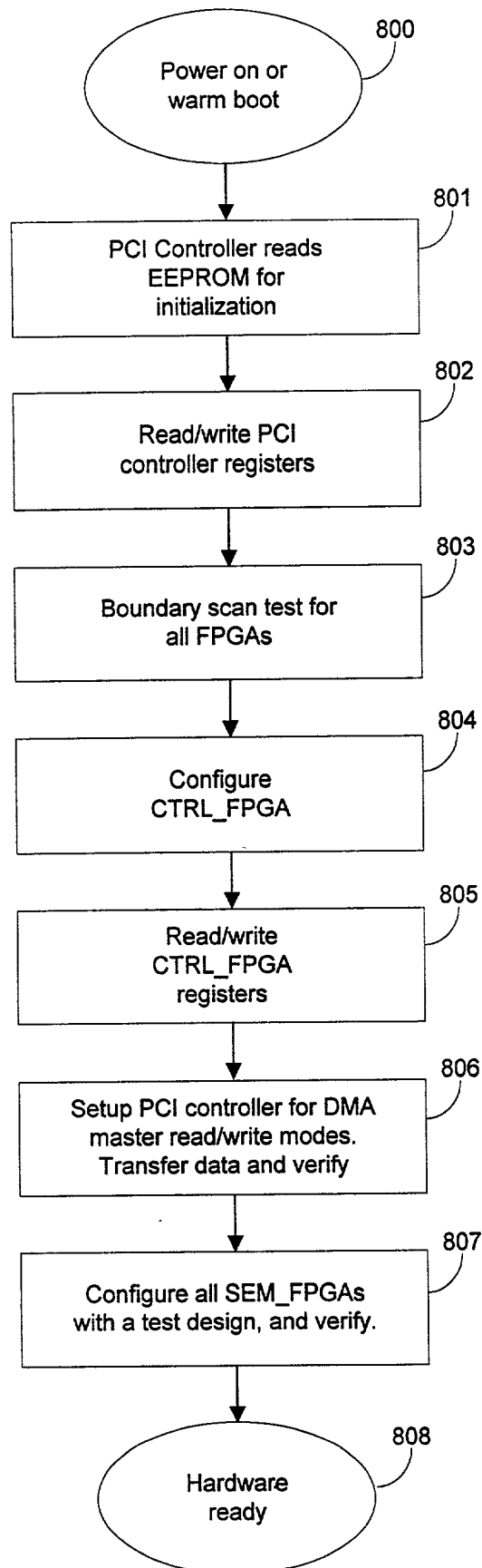


FIG. 25

```

module register (clock, reset, d, q);
input clock, d, reset;
output q;
reg q;

always@(posedge clock or negedge reset)
    if(!reset)
        q = 0;
    else
        q = d;

endmodule

module example;
    wire d1, d2, d3;
    wire q1, q2, q3;

    reg signin;
    wire sigout;
    reg clk, reset;

    register reg1 (clk, reset, d1, q1);
    register reg2 (clk, reset, d2, q2);
    register reg3 (clk, reset, d3, q3);

    assign d1 = signin ^ q3;
    assign d2 = q1 ^ q3;
    assign d3 = q2 ^ q3;
    assign sigout = q3;

    // a clock generator
    always
    begin
        clk = 0;
        #5;
        clk = 1;
        #5;
    end

    // a signal generator
    always
    begin
        #10;
        signin = $random;
    end

    // initialization
    initial
    begin
        reset = 0;
        signin = 0;
        #1;
        reset = 1;
        #5;
        $monitor($time, " %b, %b", signin, sigout);
        #1000 $finish;
    end
end module

```

FIG. 26

[illegible]

FIG. 27

```

module register (clock, reset, d, q);
input clock, d, reset;
output q;
reg q;

always@(posedge clock or negedge reset)
  if(~reset)
    q = 0;
  else
    q = d;

endmodule

```

Register Definition
900

```

module example;
  wire d1, d2, d3;
  ware q1, q2, q3;

```

wire interconnection info
907

```

reg signin;
wire sigout;
reg clk, reset;

```

Test-bench input -- 908
Test-bench output -- 909

```

S1 register reg 1 (clk, reset, d1, q1);
S2 register reg 2 (clk, reset, d2, q2);
S3 register reg 3 (clk, reset, d3, q3);

```

Register component
901

```

S4 assign d1 = signin ^ q3;
S5 assign d2 = q1 ^ 3;
S6 assign d3 = q2 ^ q3;
S7 assign signout = q3;

```

Combinational component
902

```

S8 {
  // a clock generator
  always
  begin
    clk = 0;
    #5;
    clk = 1;
    #5;
  end
}

```

Clock component
903

```

S9 {
  // a signal generator
  always
  begin
    #10;
    signin = $random;
  end
}

```

Test-bench component (Driver)
904

```

S10 {
  // initialization
  initial
  begin
    reset = 0;
    signin = 0;
    #1;
    reset = 1;
    #5;
  end
}

```

Test-bench component (initialization)
905

```

S11 {
  $monitor($time, "%b, %b", signin, sigout);
  #1000 $finish;
}
end
end module

```

Test-bench component (monitor)
906

FIG. 28

SIGNAL NETWORK ANALYSIS

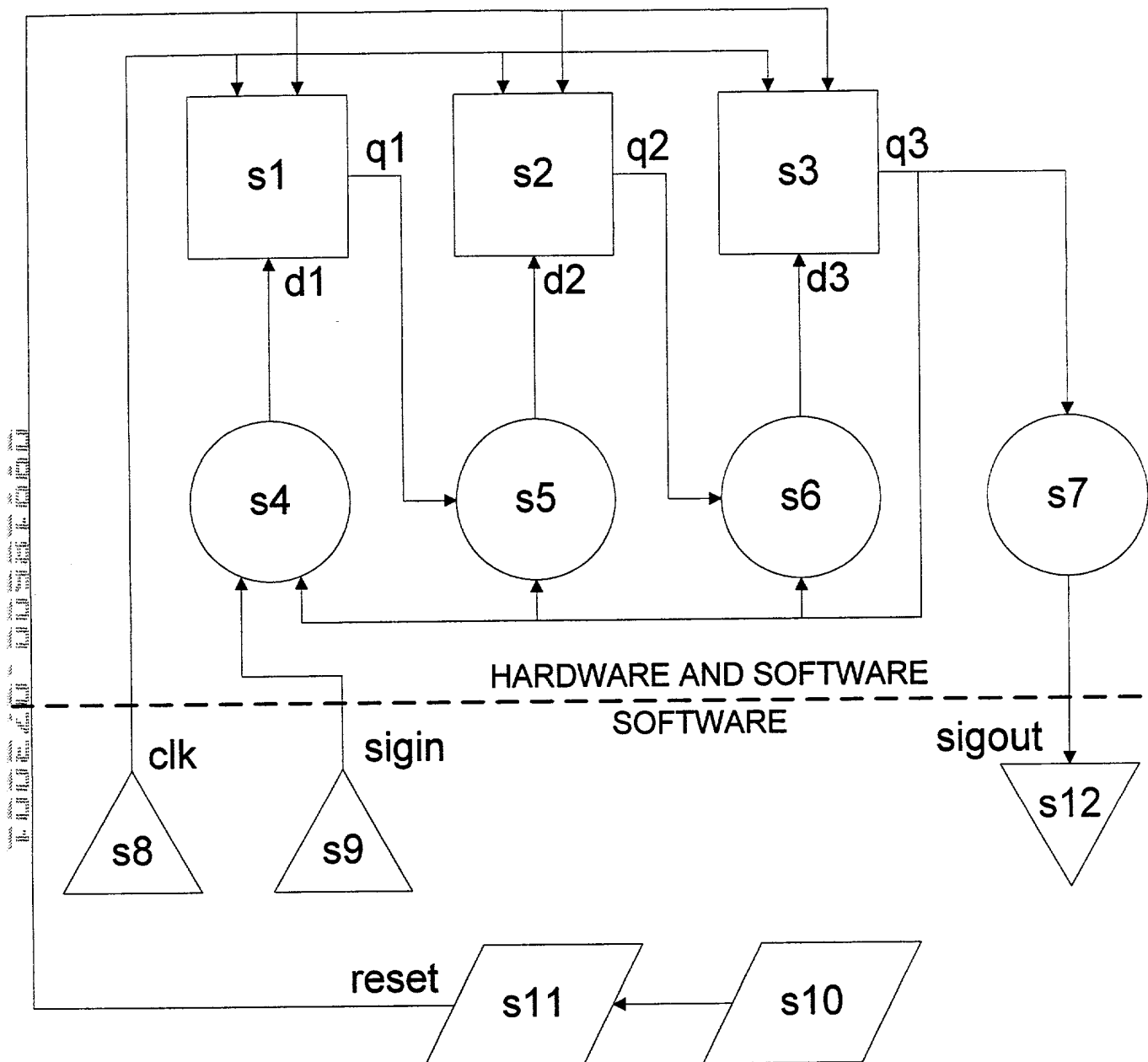


FIG. 29

SOFTWARE/HARDWARE PARTITION RESULT

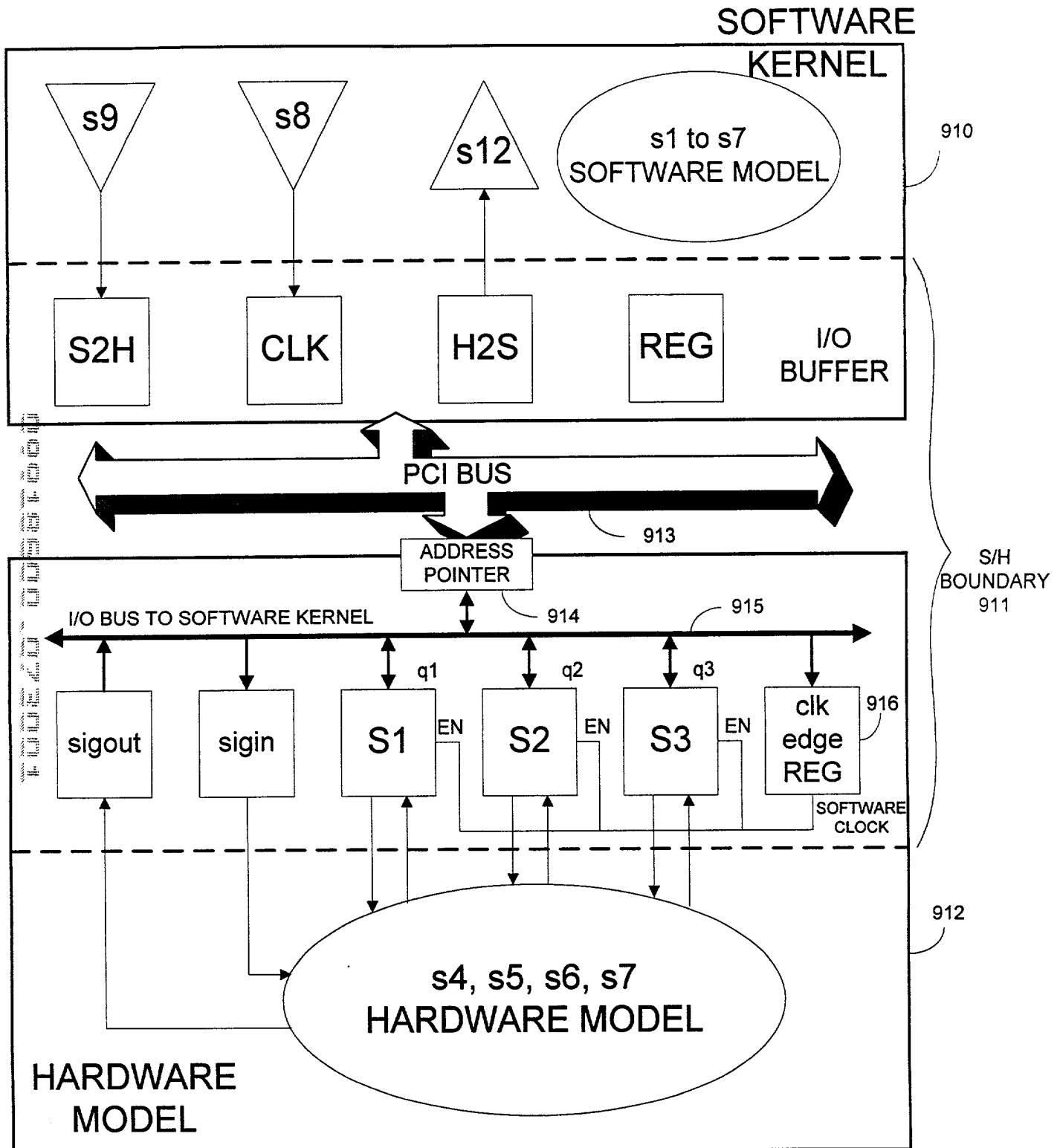


FIG. 30

HARDWARE MODEL

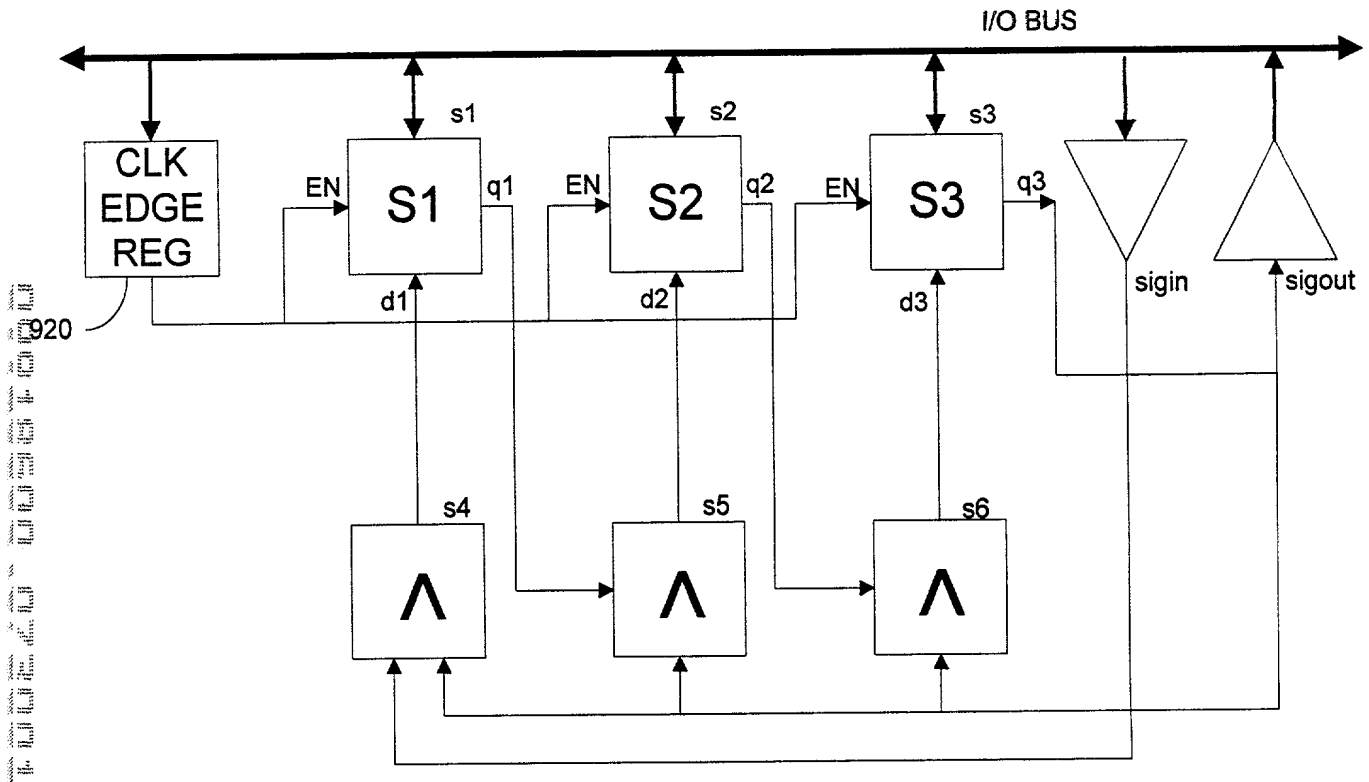
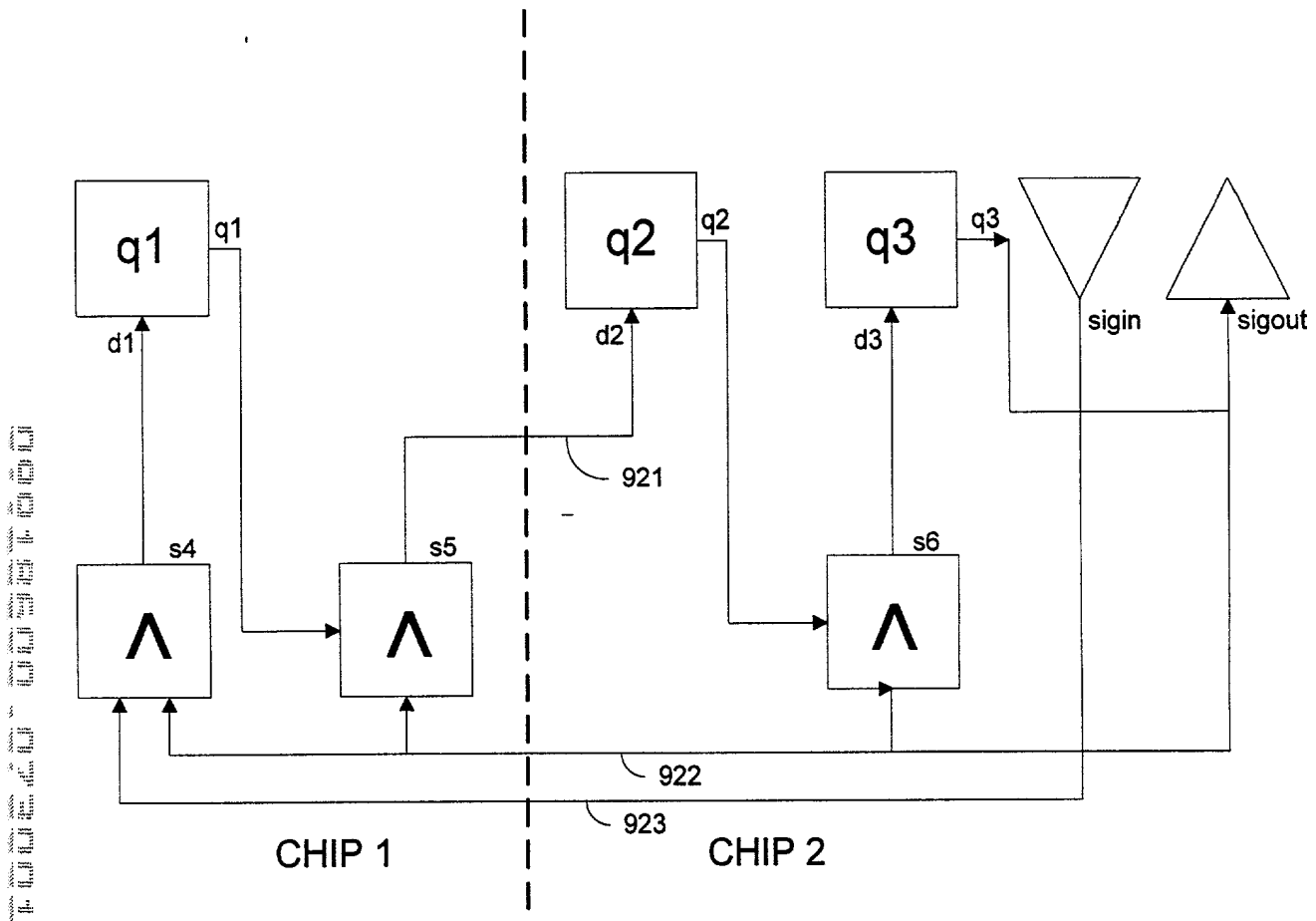


FIG. 31

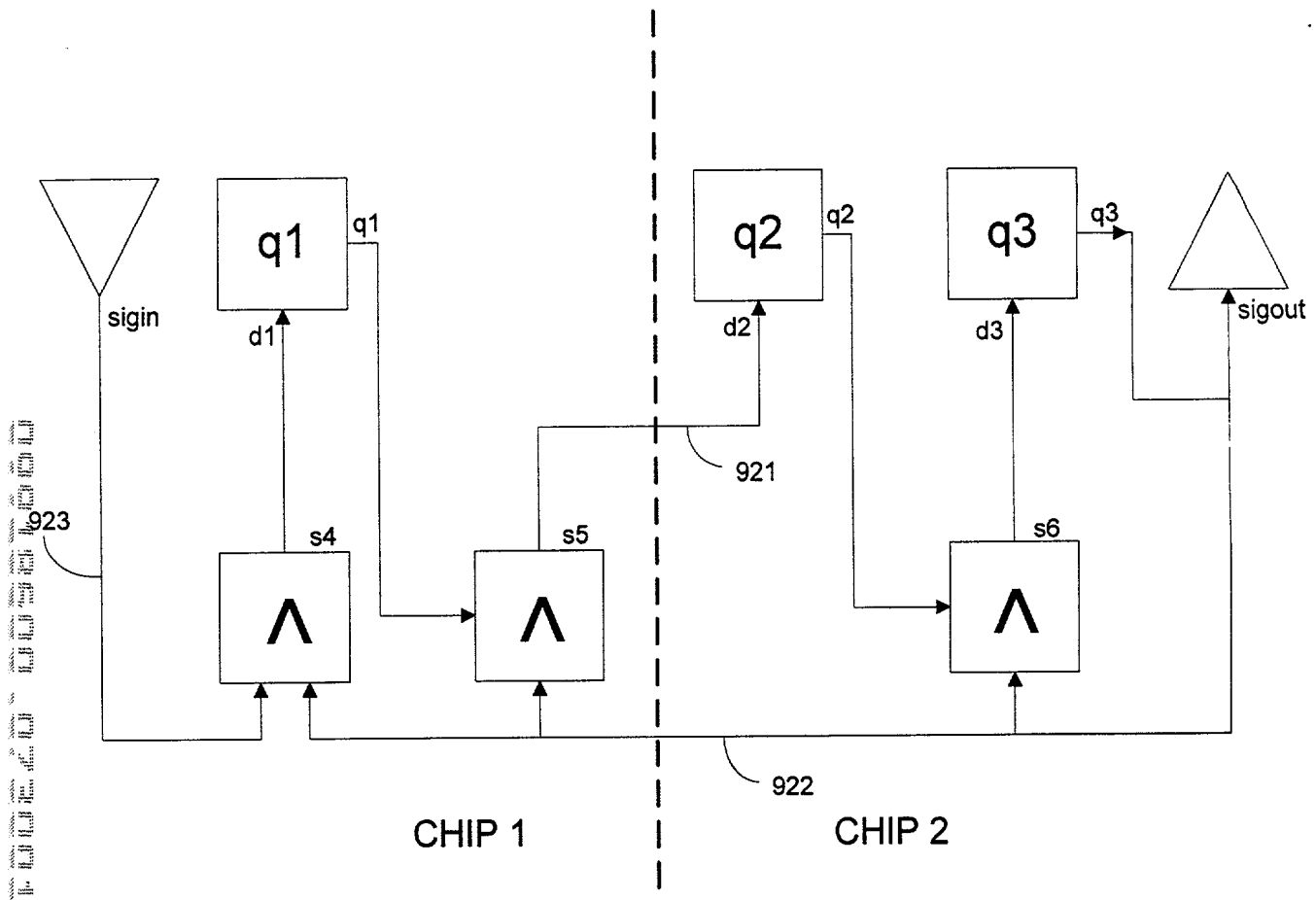
PARTITION RESULT #1



(IGNORE I/O AND CLOCK EDGE REGISTER)

FIG. 32

PARTITION RESULT #2



(IGNORE I/O AND CLOCK EDGE REGISTER)

FIG. 33

LOGIC PATCHING

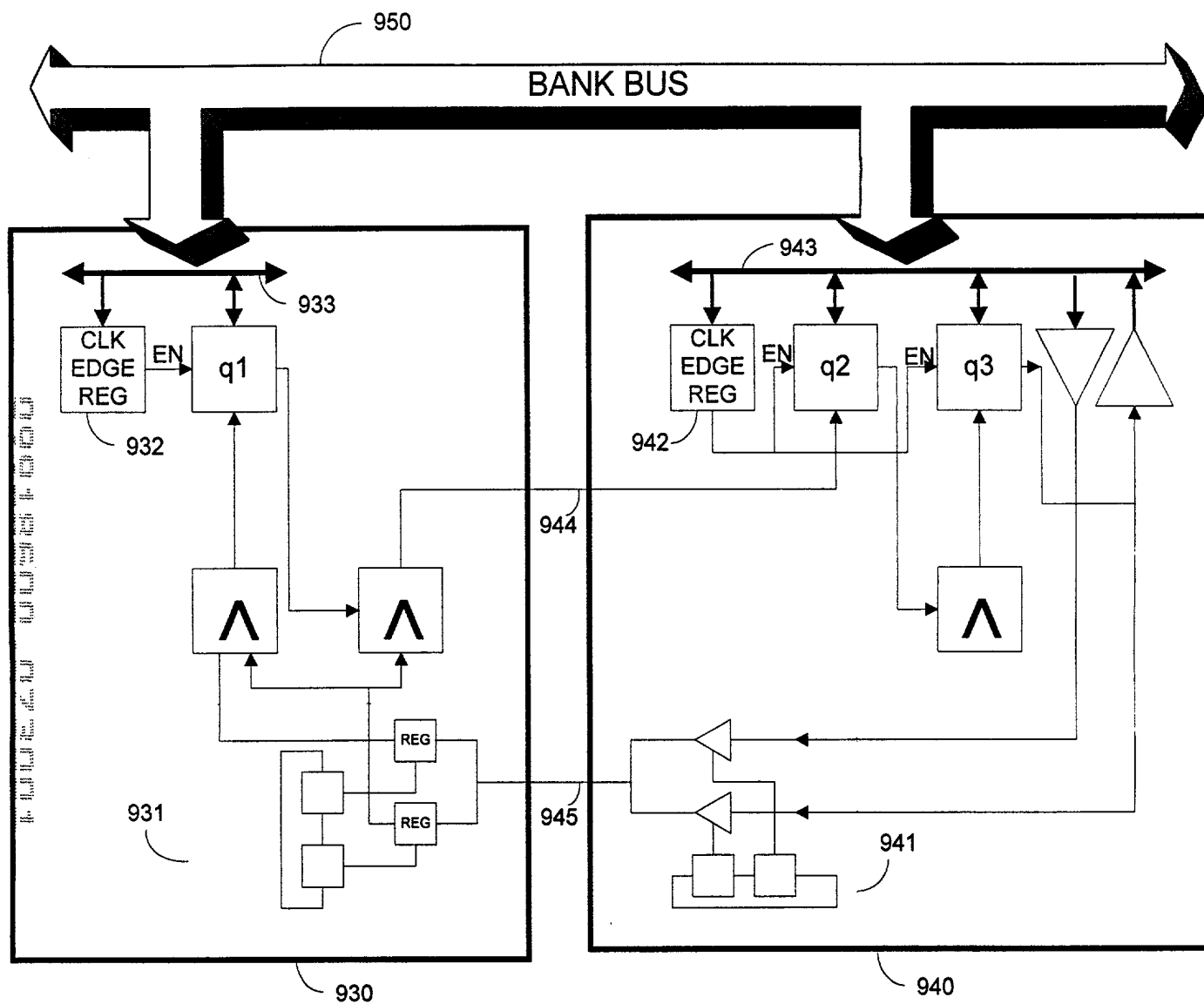


FIG. 34

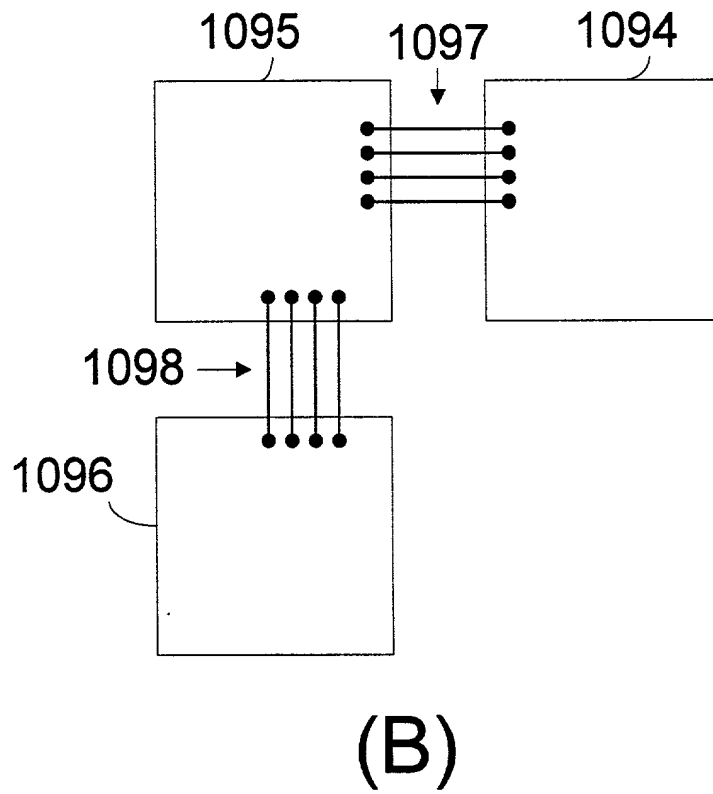
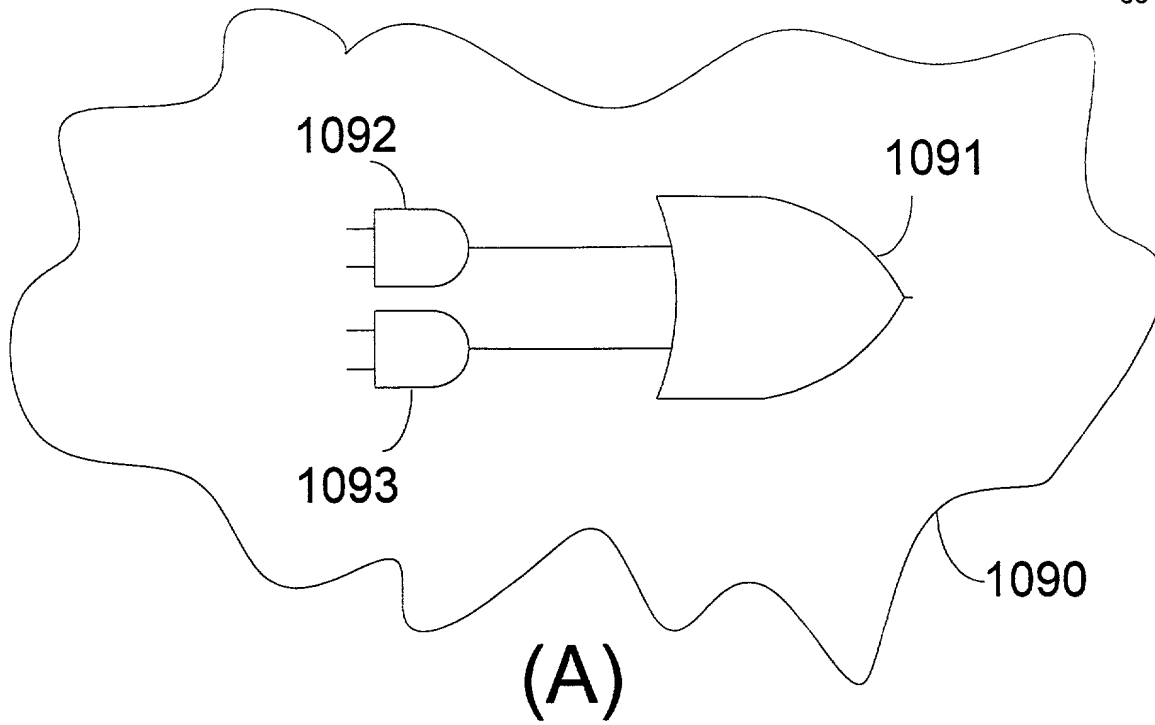
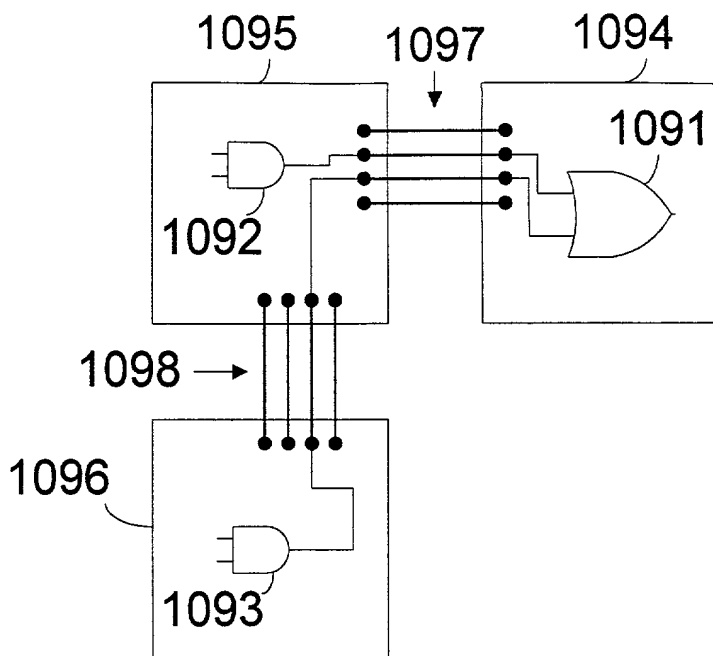
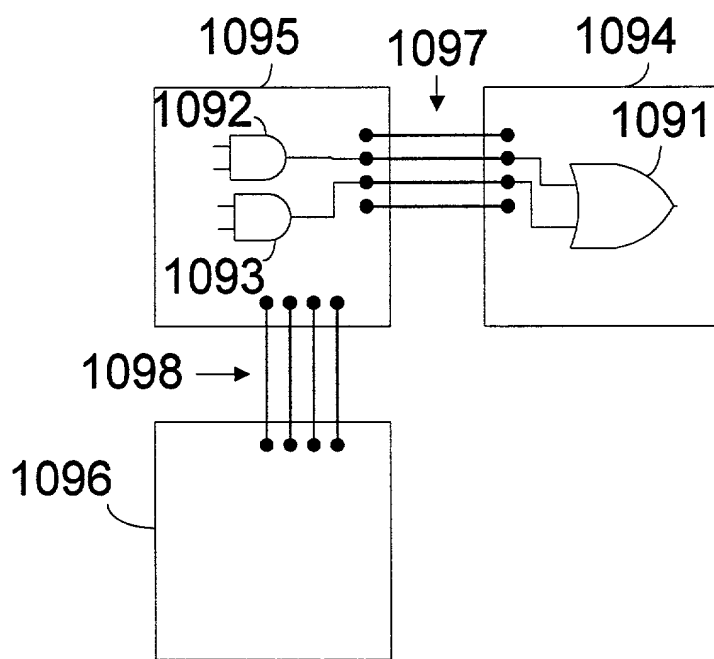


FIG. 35



(C)

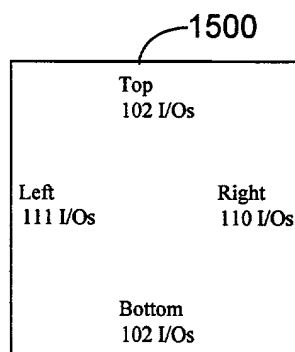


(D)

FIG. 35

I/O PIN OVERVIEW OF FPGA LOGIC DEVICE

FPGA : 10K130V, 10K250V with 599-pin PGA package



**425 Interconnect I/O
pins**

45 Dedicated I/O pins:

GCLK, FD_BUS[31..0], F_RD, F_WR,
DATA_XSFR, SHIFTIN, SHIFTOUT,
SPACE[2..0], EVAL, EV_REQ_N,
DEV_OE, DEV_CLRN

FIG. 36

FPGA INTERCONNECT BUSES

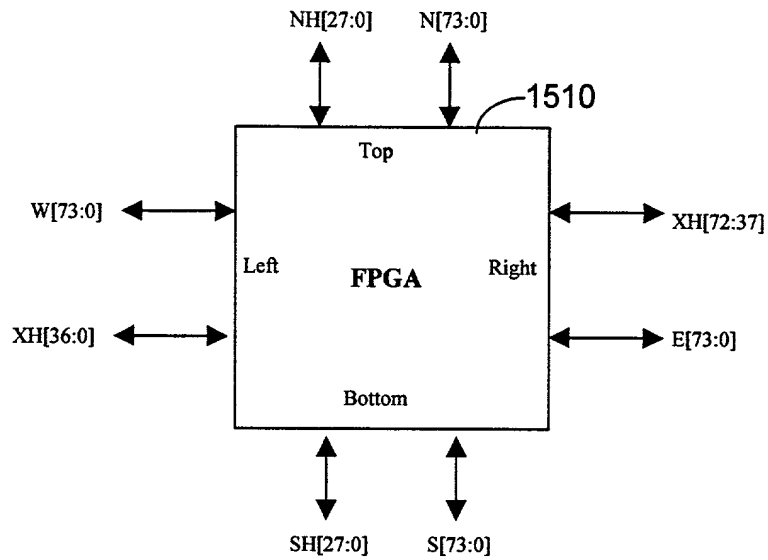


FIG. 37

BOARD CONNECTION - SIDE VIEW

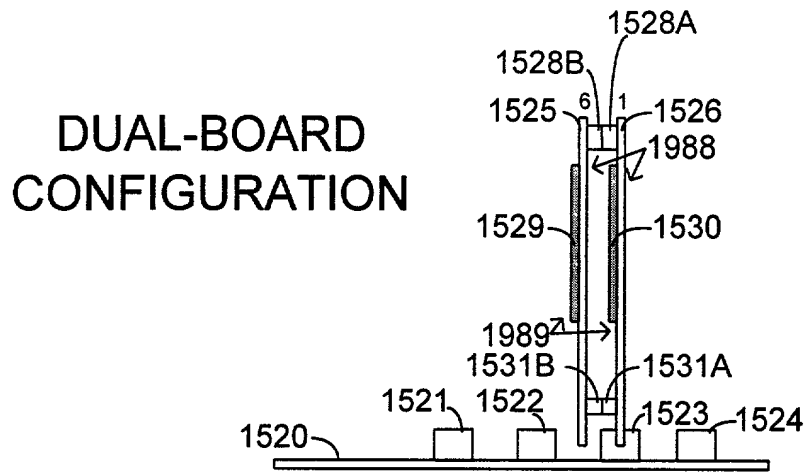


FIG. 38(A)

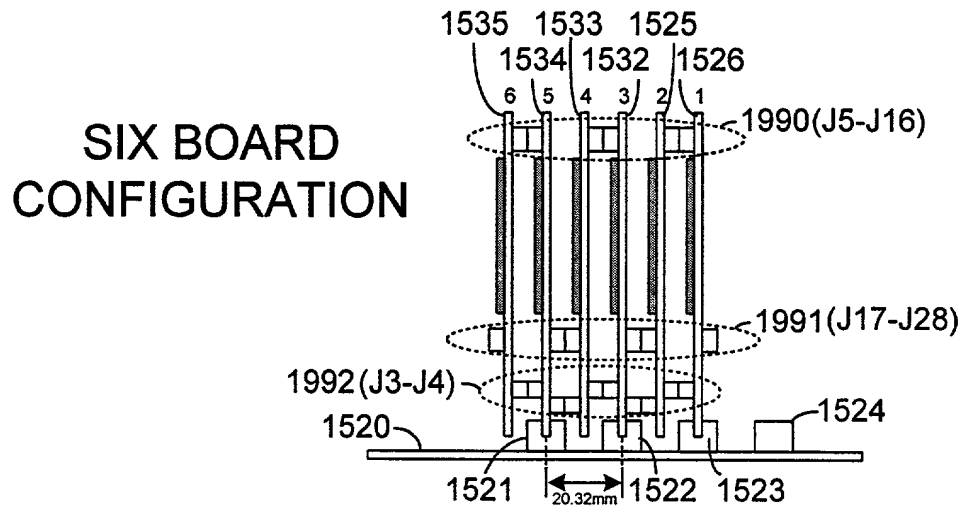


FIG. 38(B)

SIX-BOARD CONFIGURATION DIRECT-NEIGHBOR AND ONE-HOP FPGA ARRAY – X TORUS, Y MESH

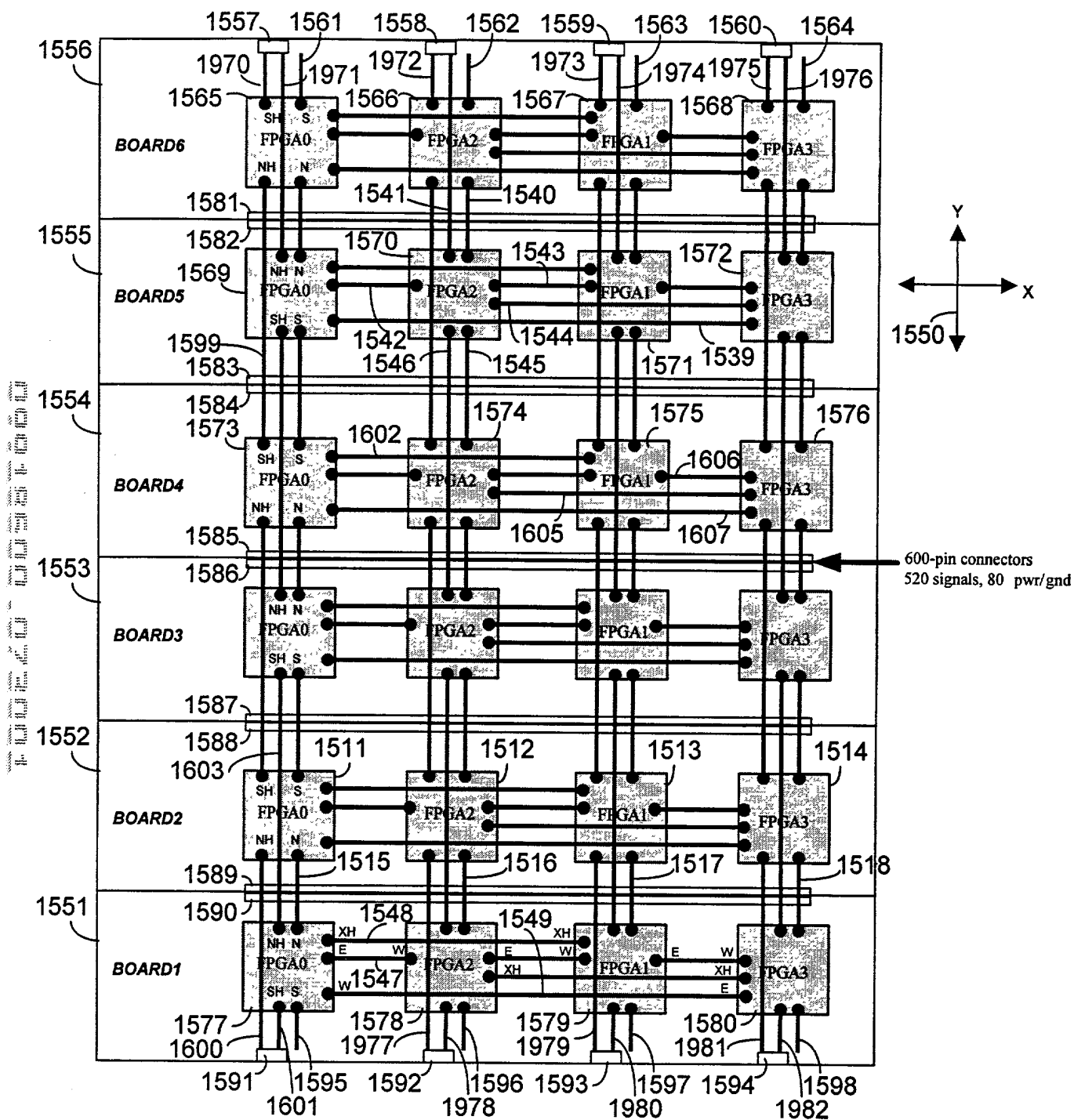


FIG. 39

FPGA ARRAY CONNECTION BETWEEN BOARDS

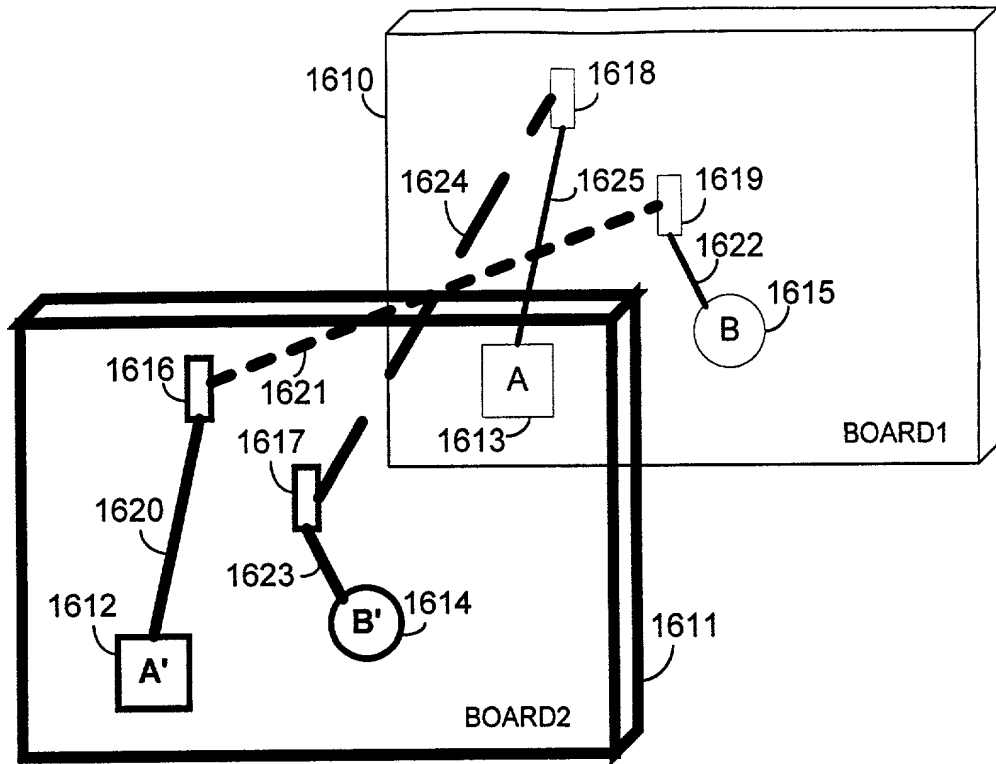


FIG. 40(A)

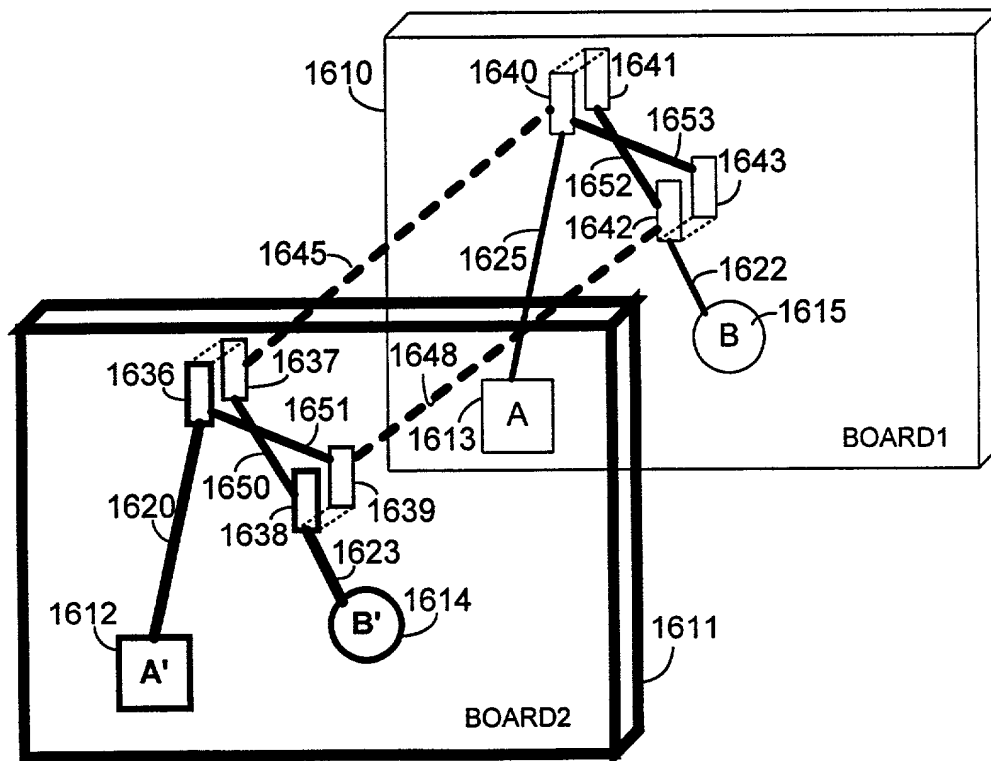


FIG. 40(B)

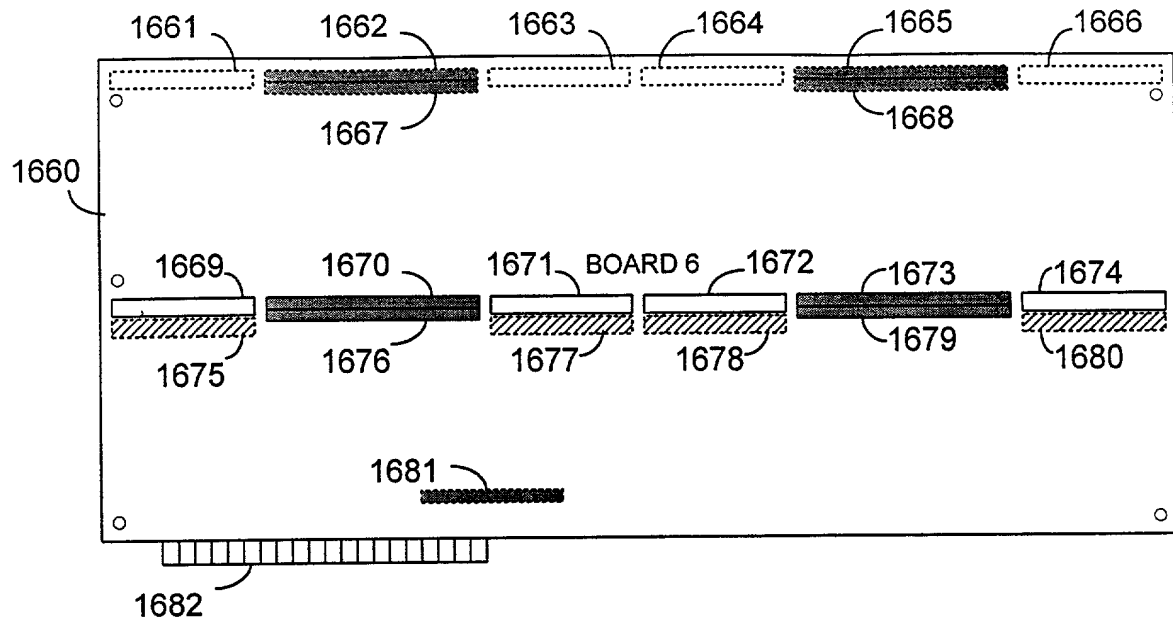


FIG. 41(A)

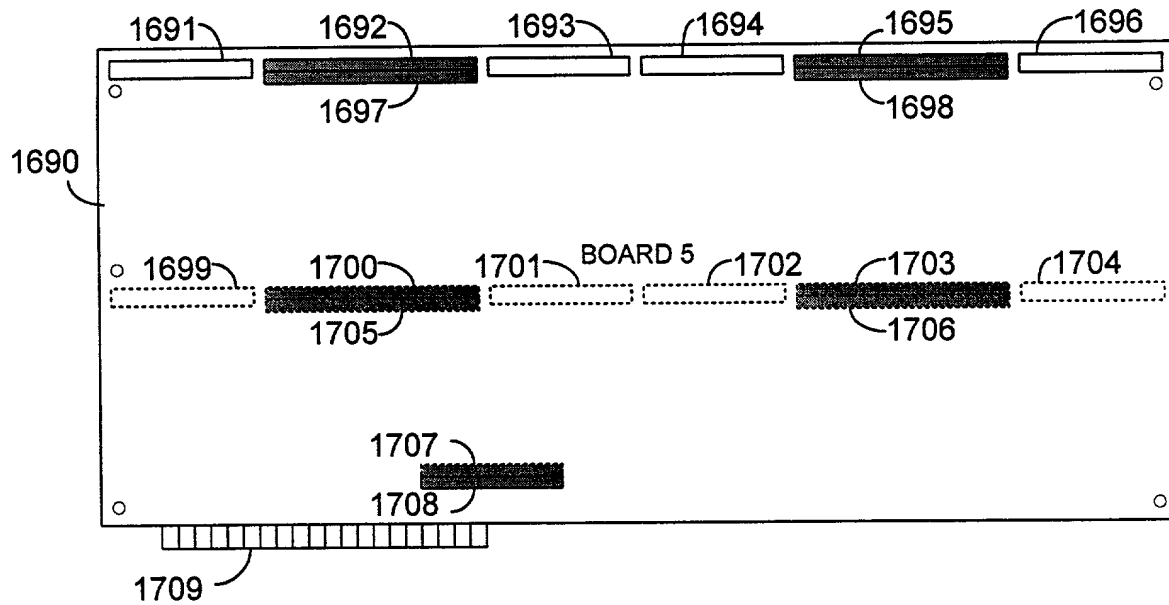


FIG. 41(B)

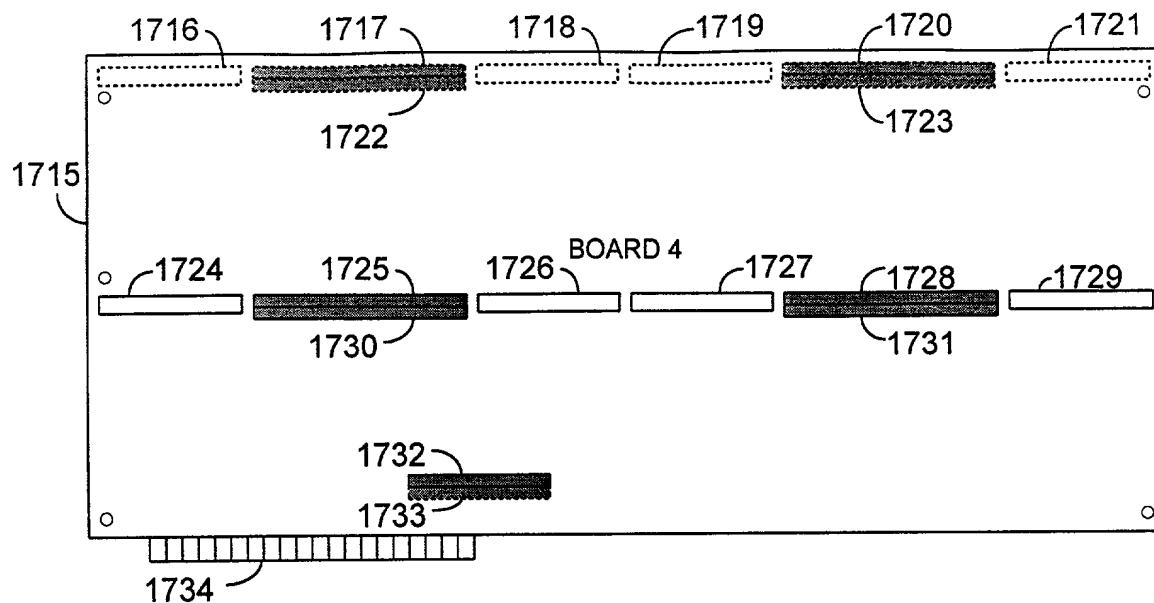


FIG. 41(C)

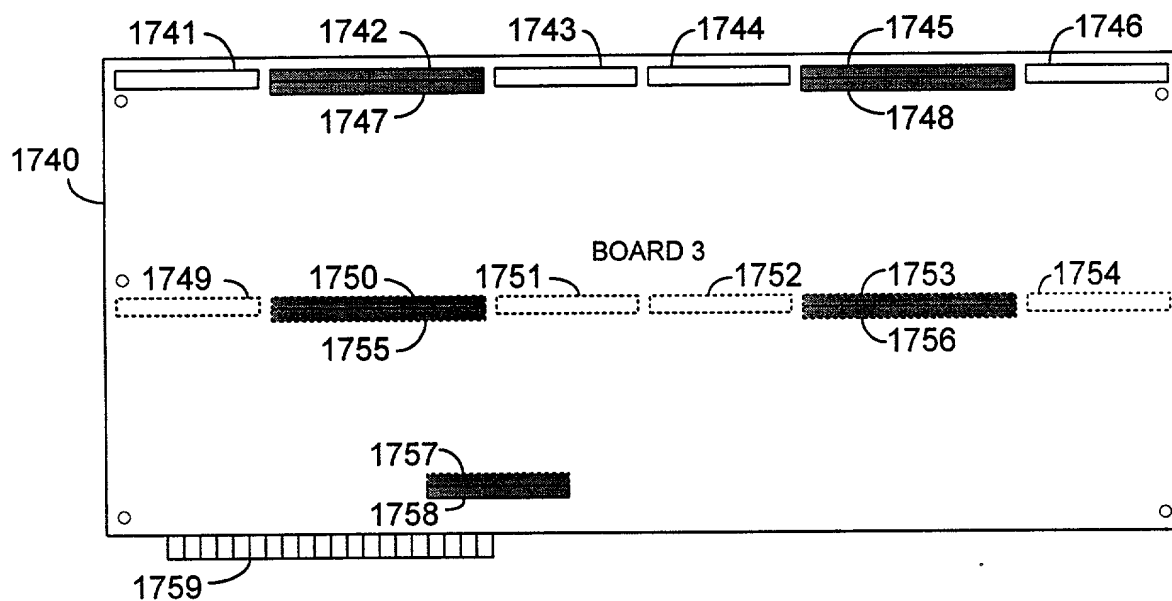


FIG. 41(D)

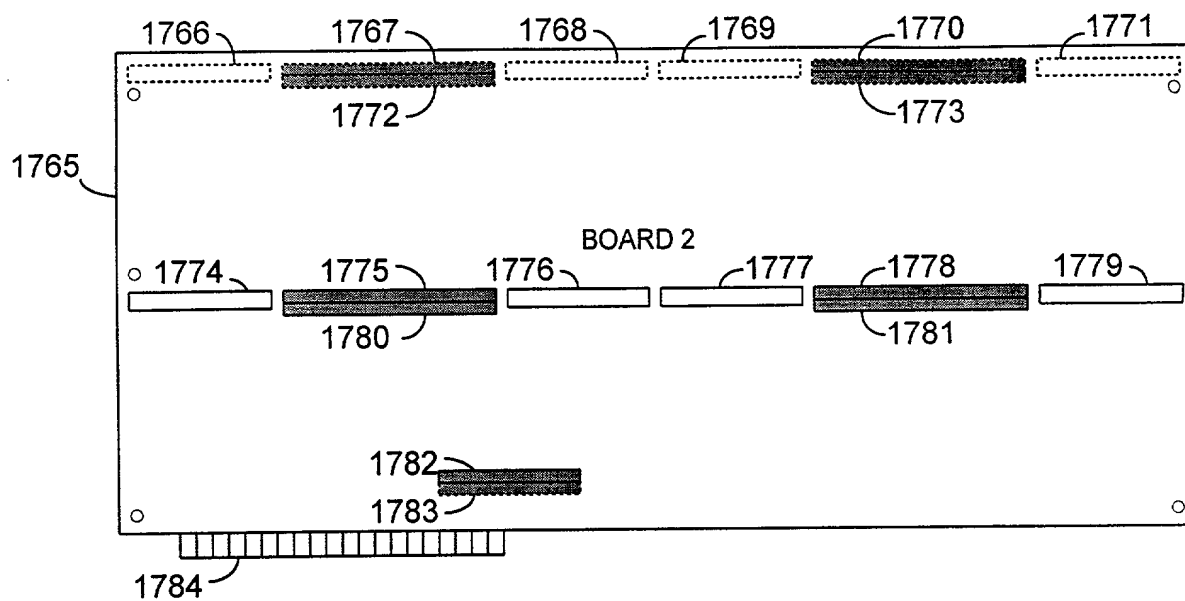


FIG. 41(E)

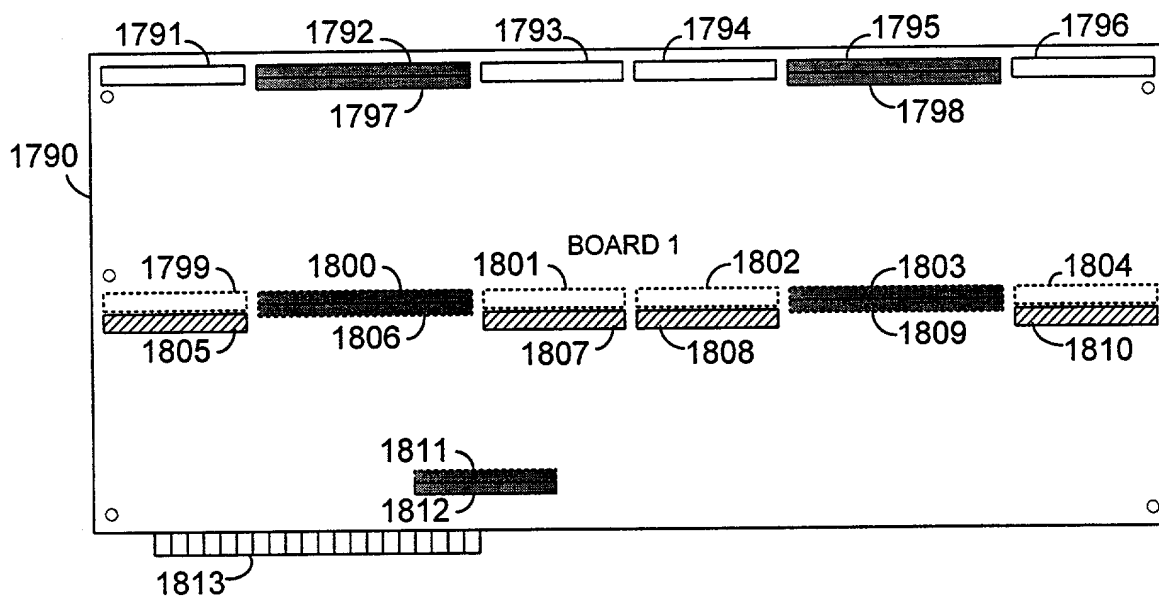


FIG. 41(F)

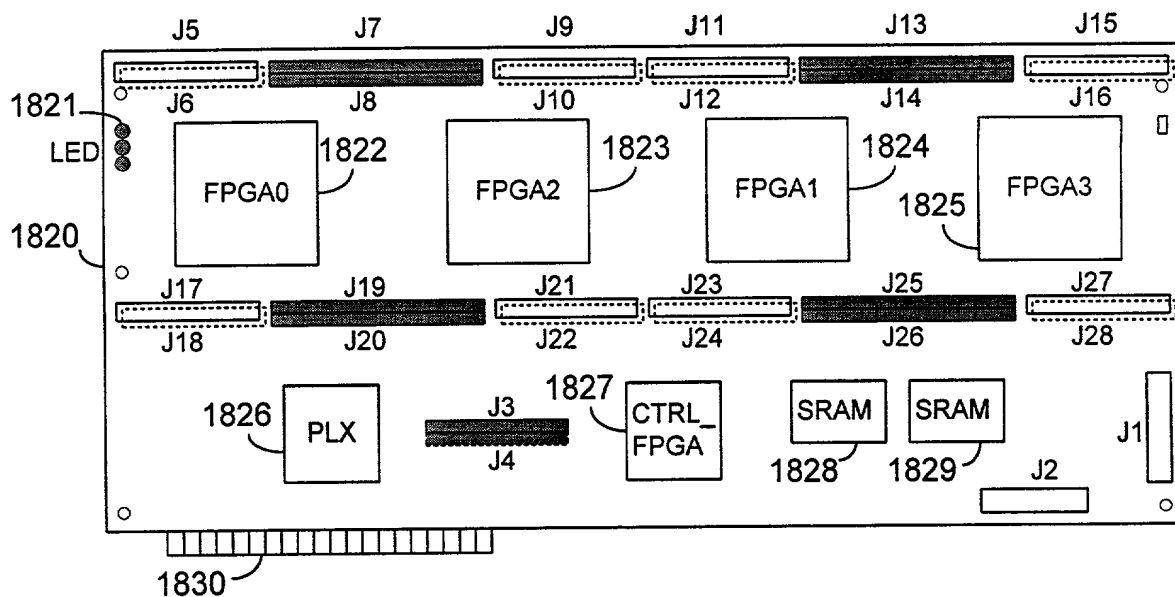


FIG. 42

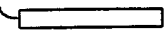
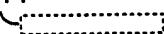



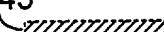
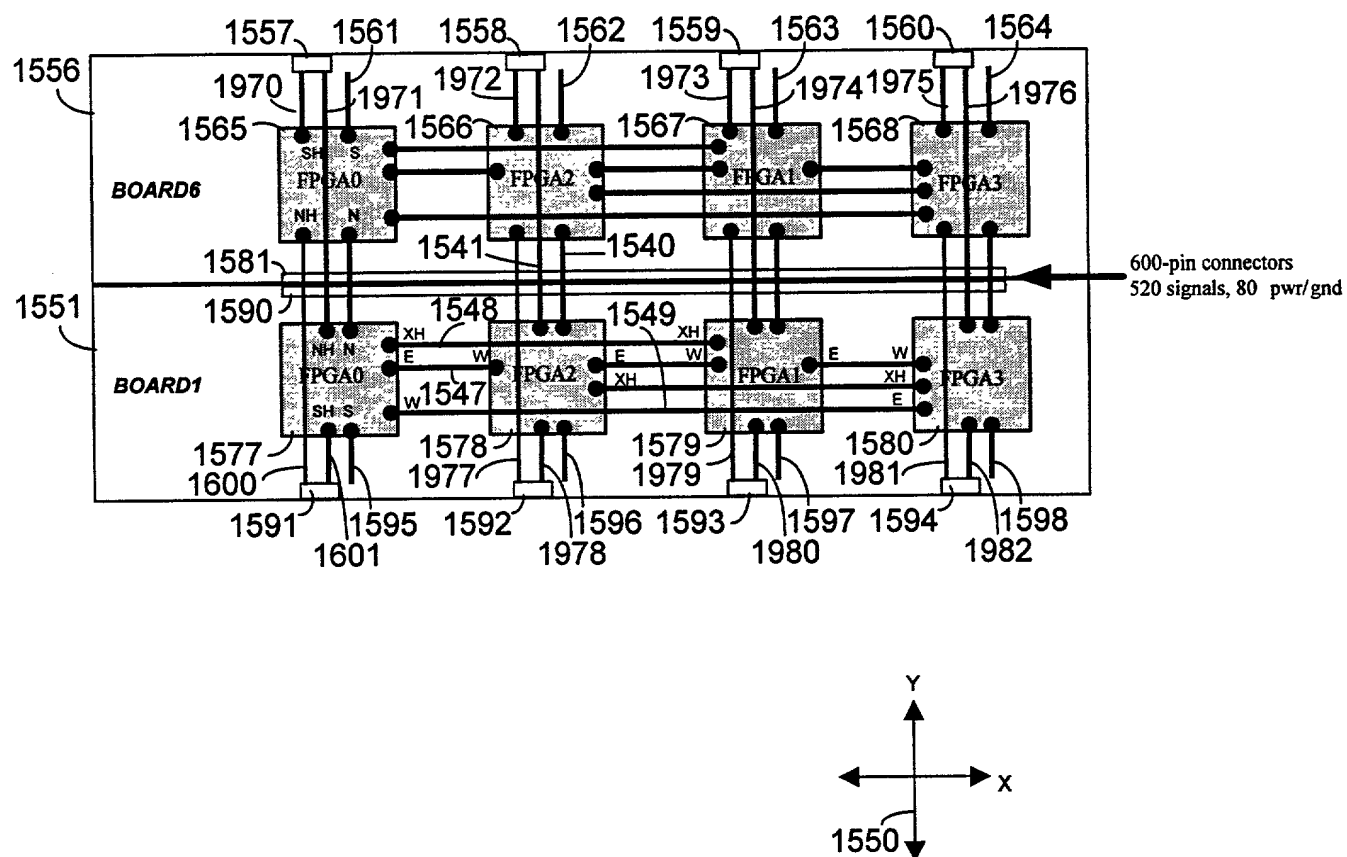
- 1840  2x30 Header, SMD, component side
- 1841  2x30 Receptacle, SMD, solder side
- 1842  2x45, 2x30 Header, thru hole, component side
- 1843  2x45, 2x30 Receptacle, thru hole, solder side
- 1844  R-pack, SMD, component side
- 1845  R-pack, SMD, solder side

FIG. 43

FIG. 44



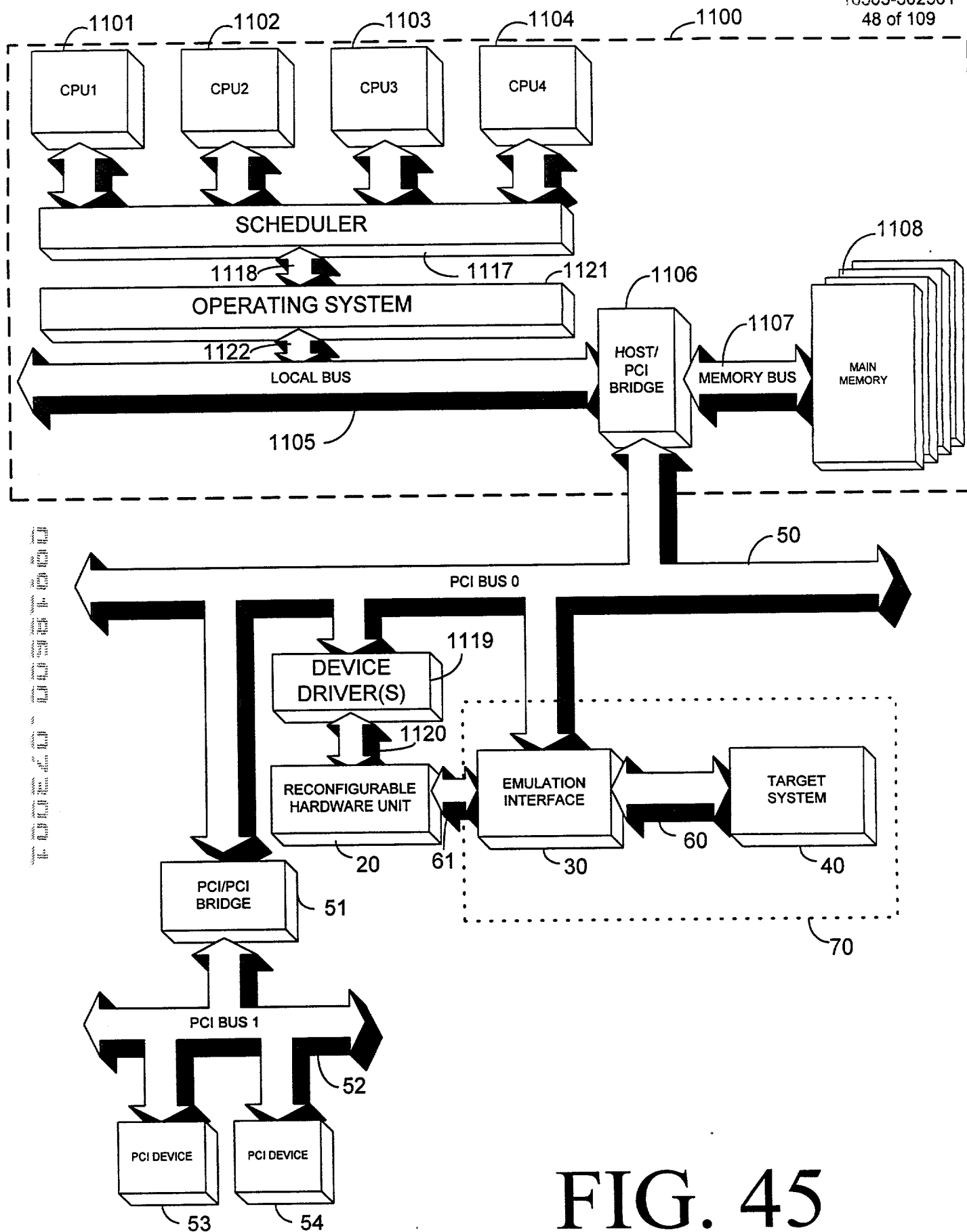


FIG. 45

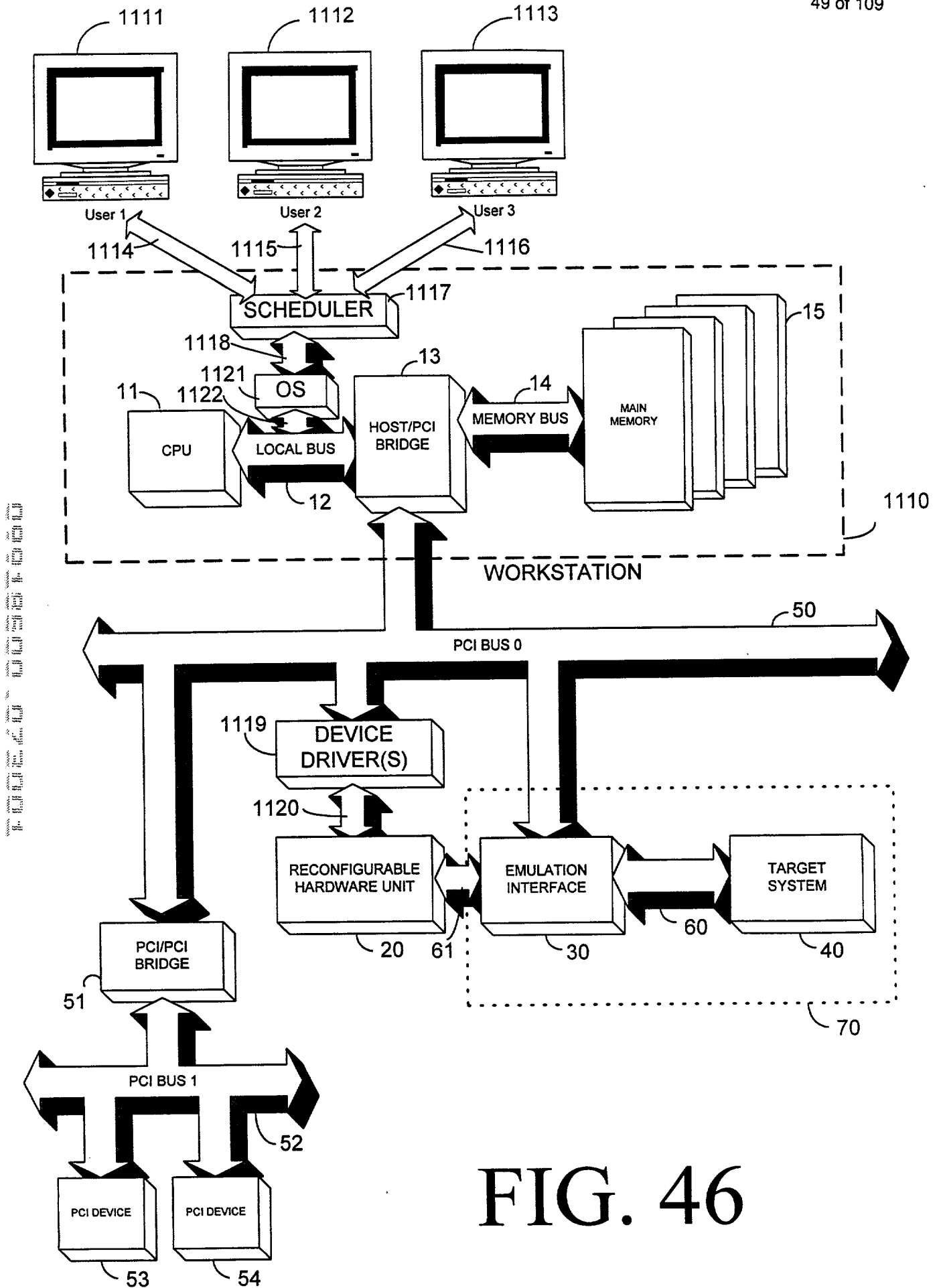


FIG. 46

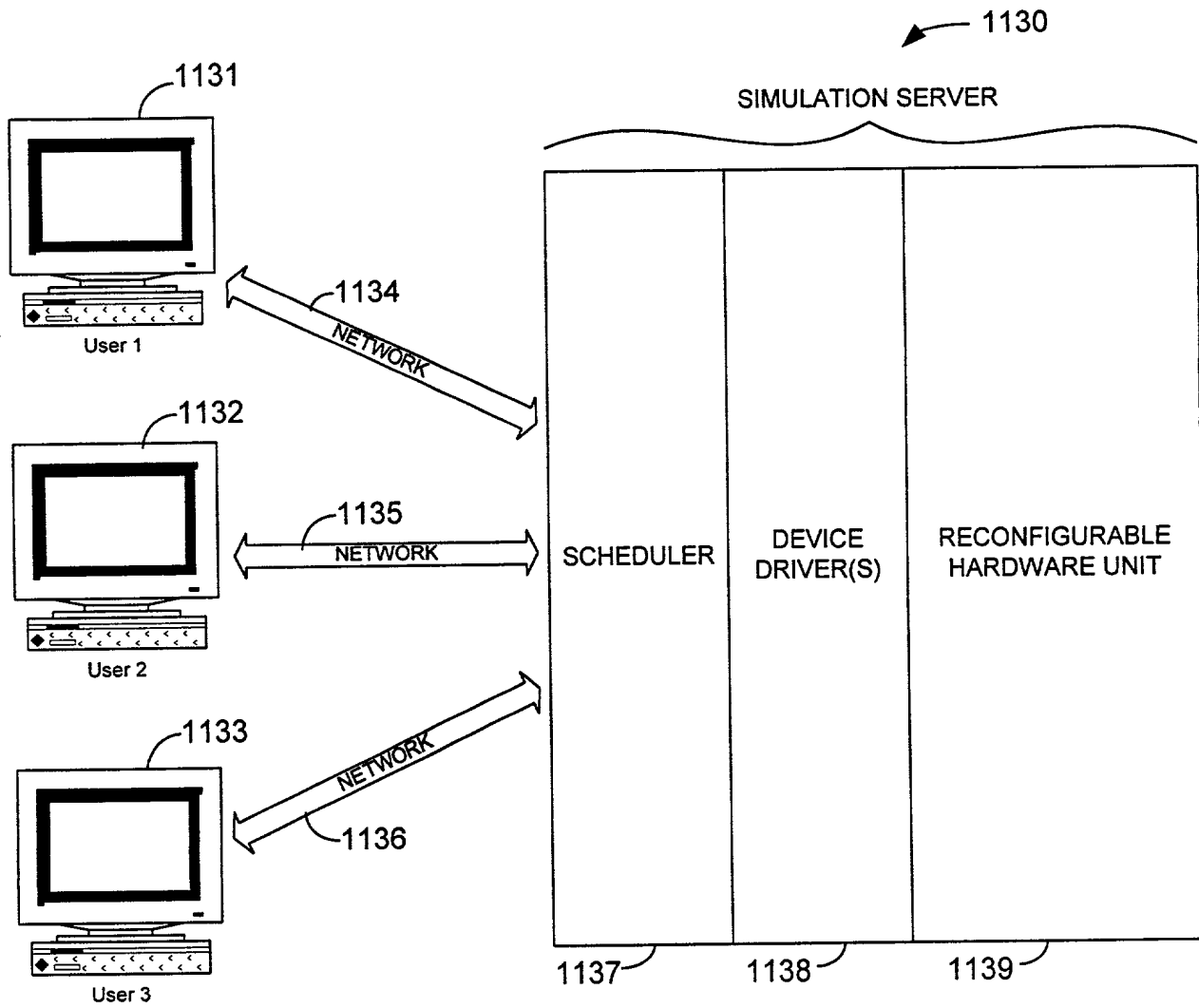


FIG. 47

SIMULATION SERVER ARCHITECTURE

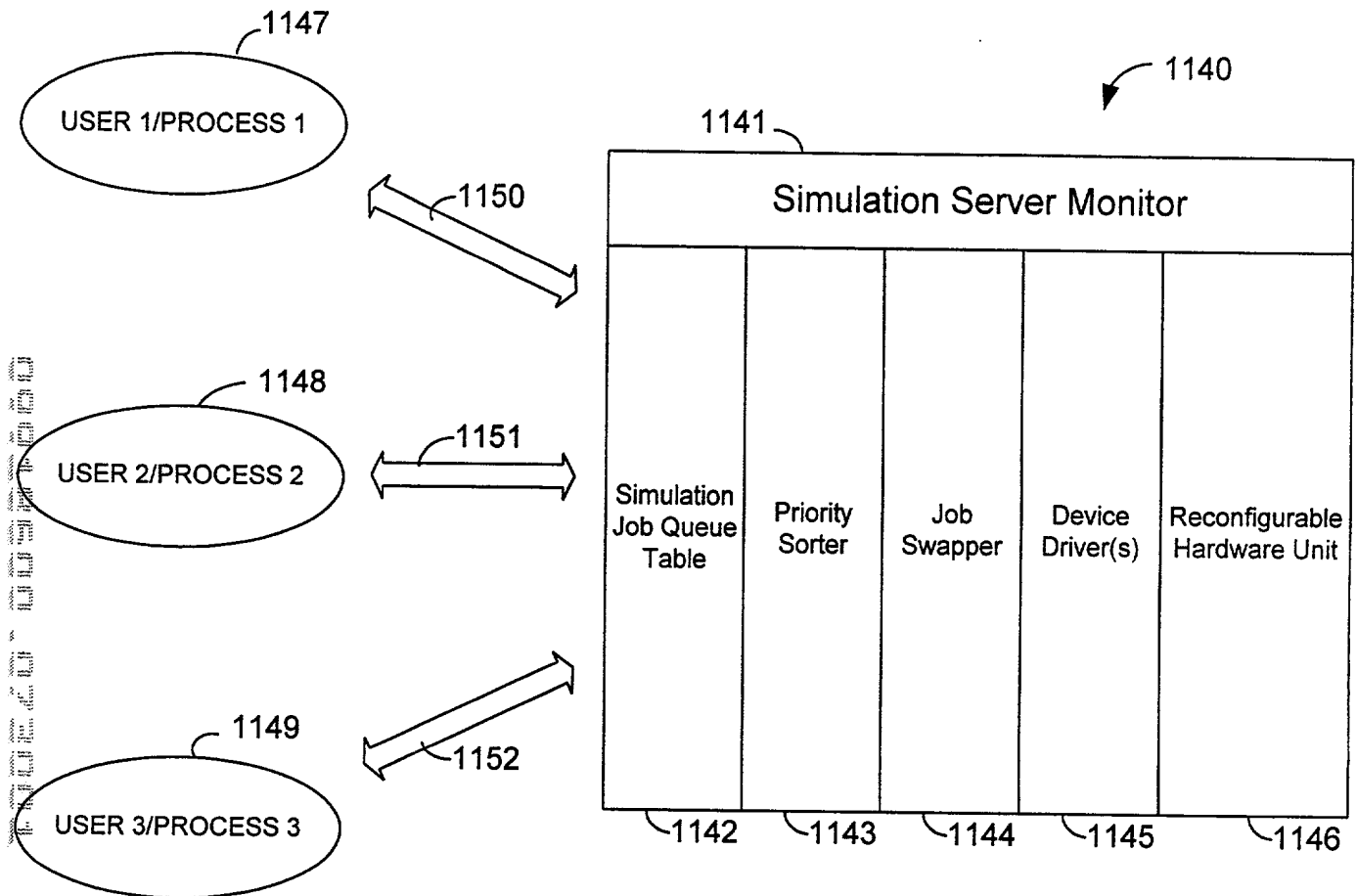


FIG. 48

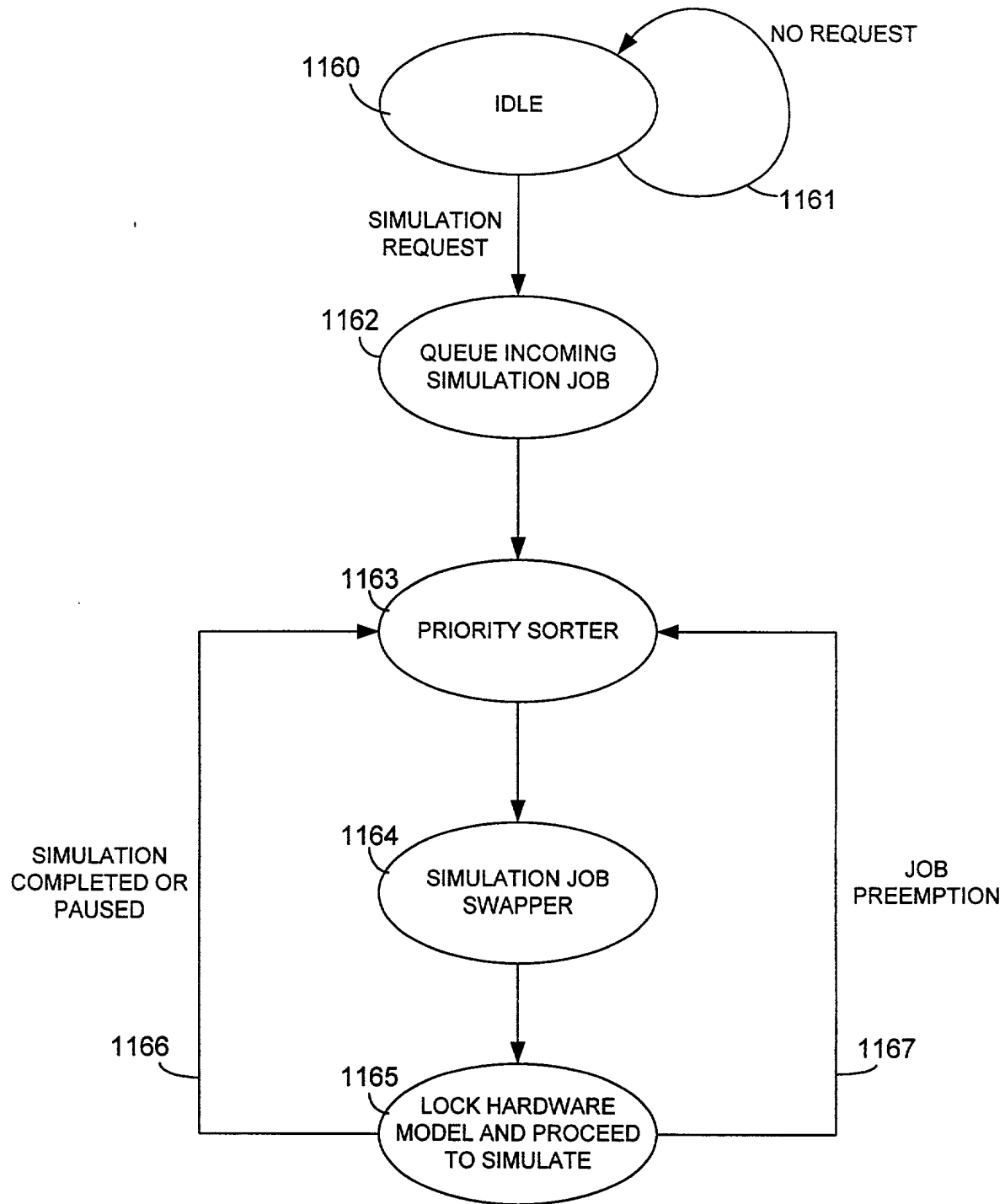


FIG. 49

JOB SWAPPER

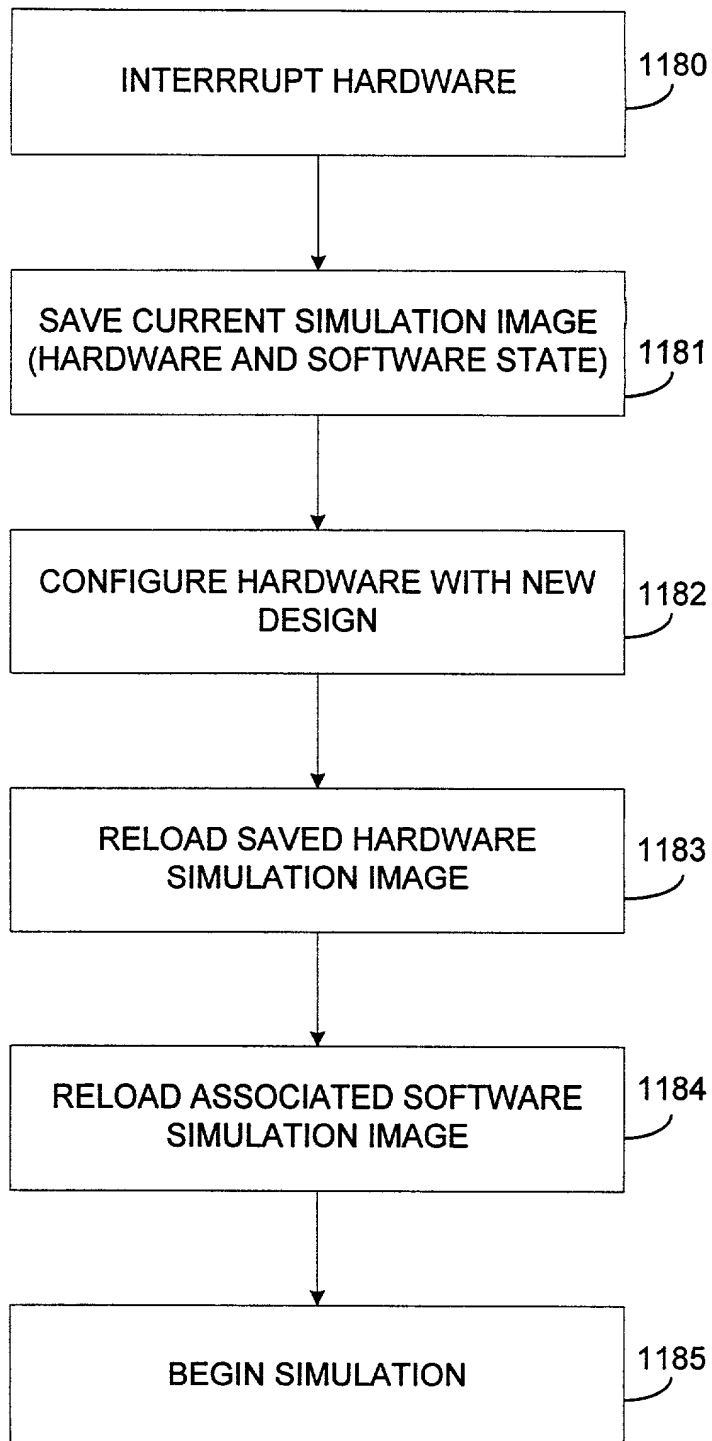


FIG. 50

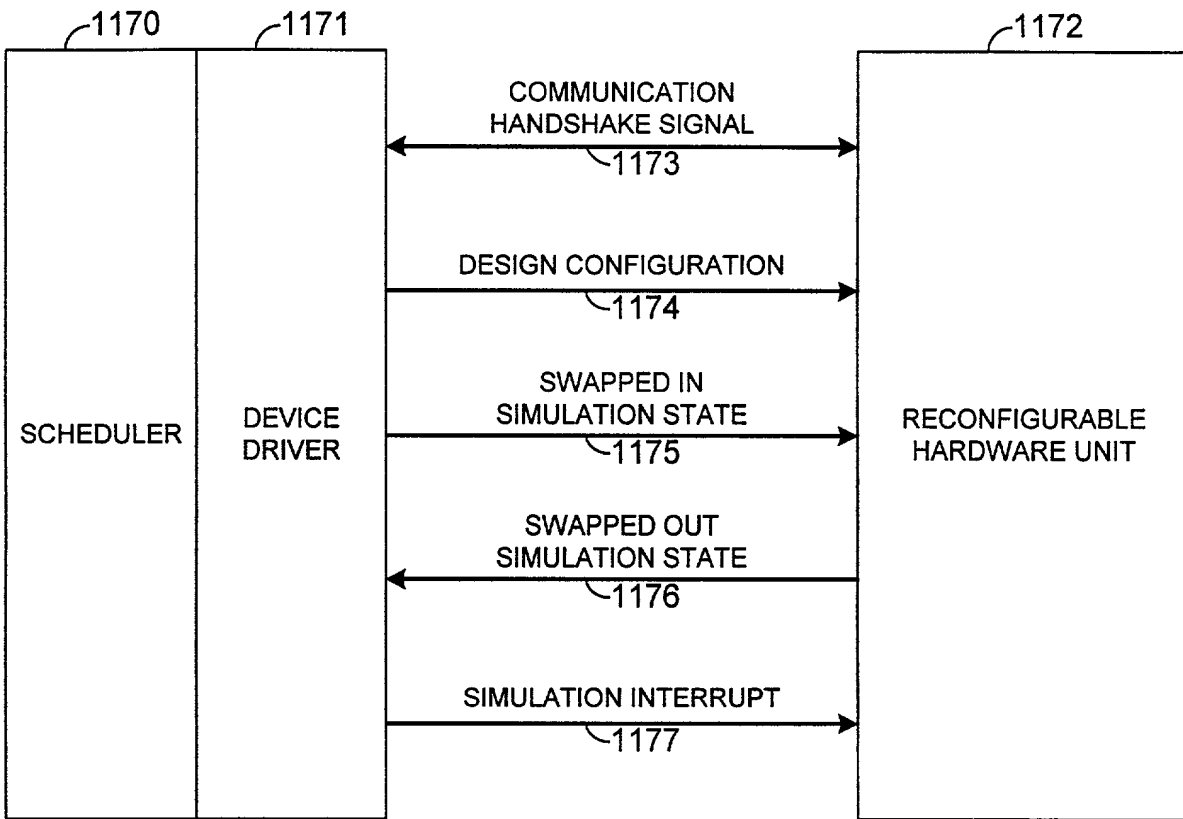
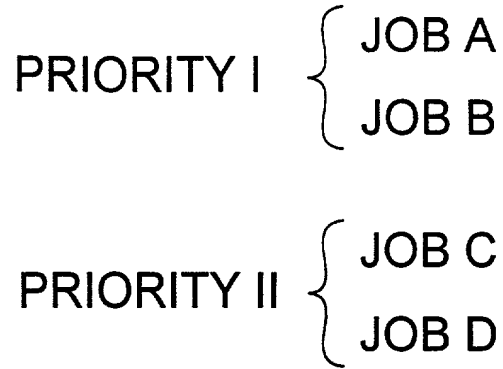


FIG. 51



TIME-SHARED HARDWARE USAGE:

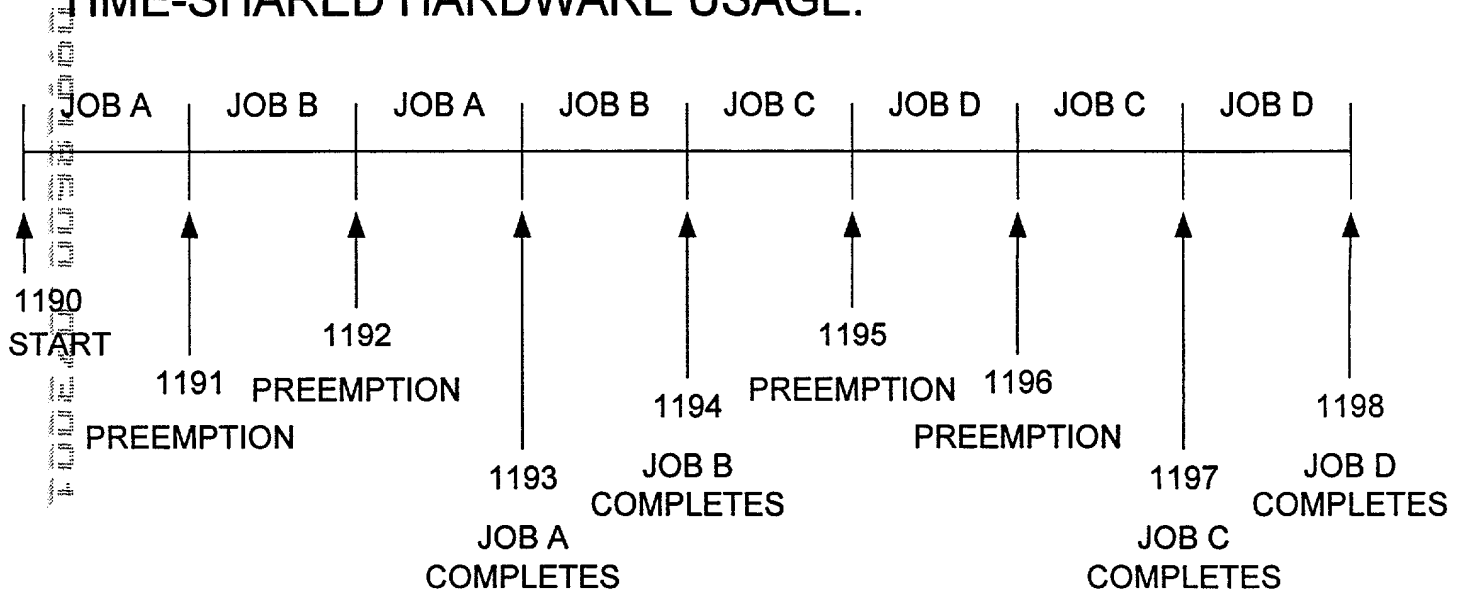


FIG. 52

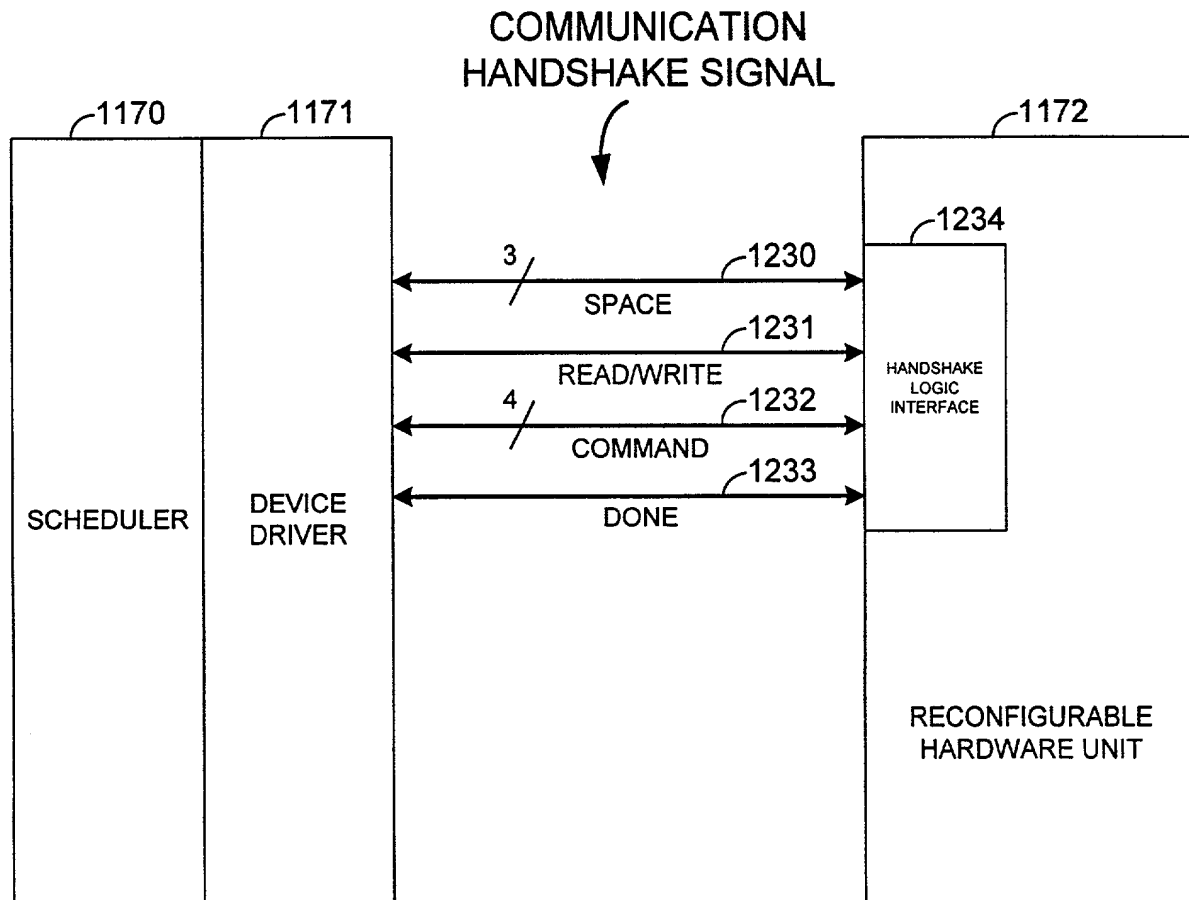


FIG. 53

COMMUNICATION HANDSHAKE PROTOCOL

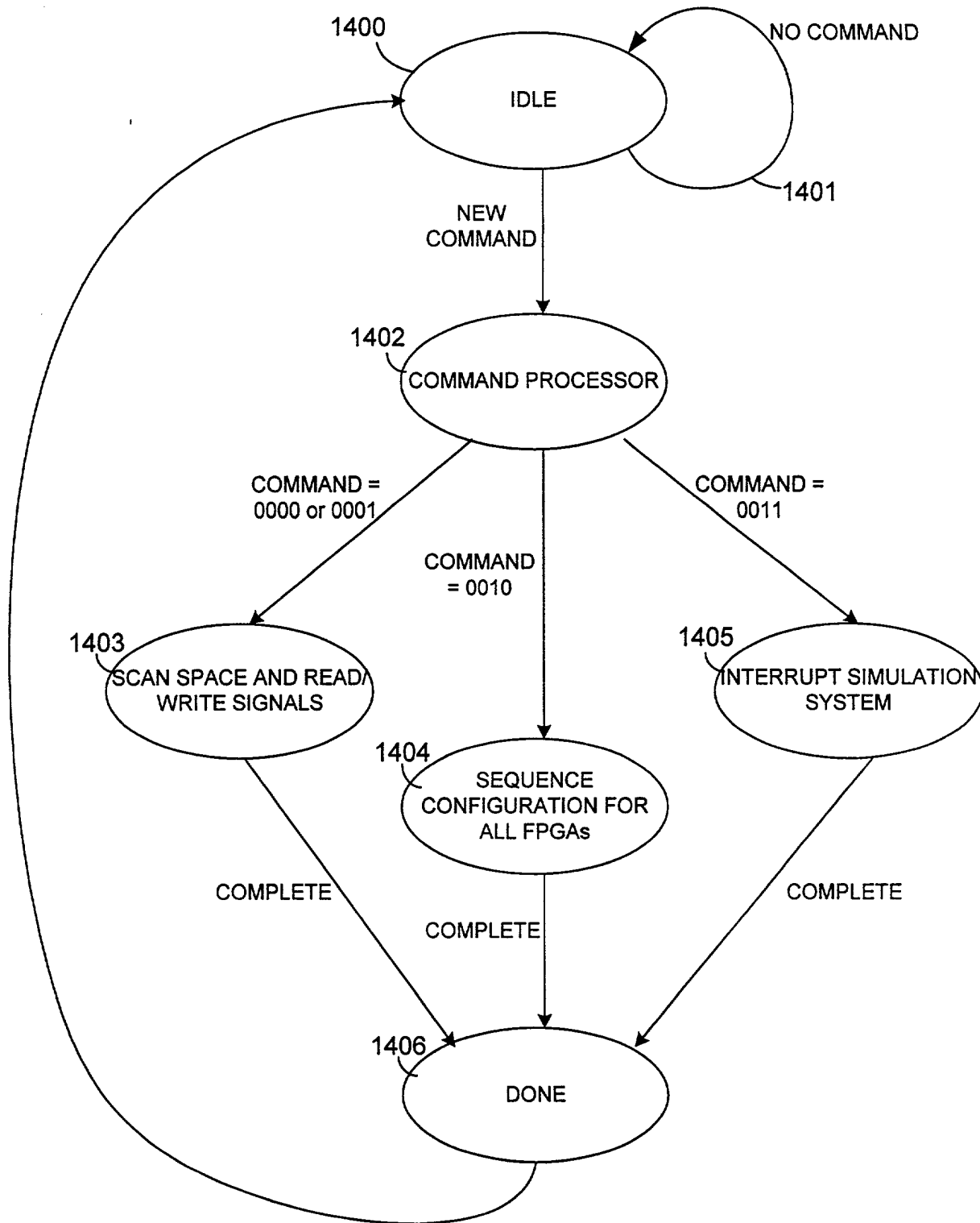


FIG. 54

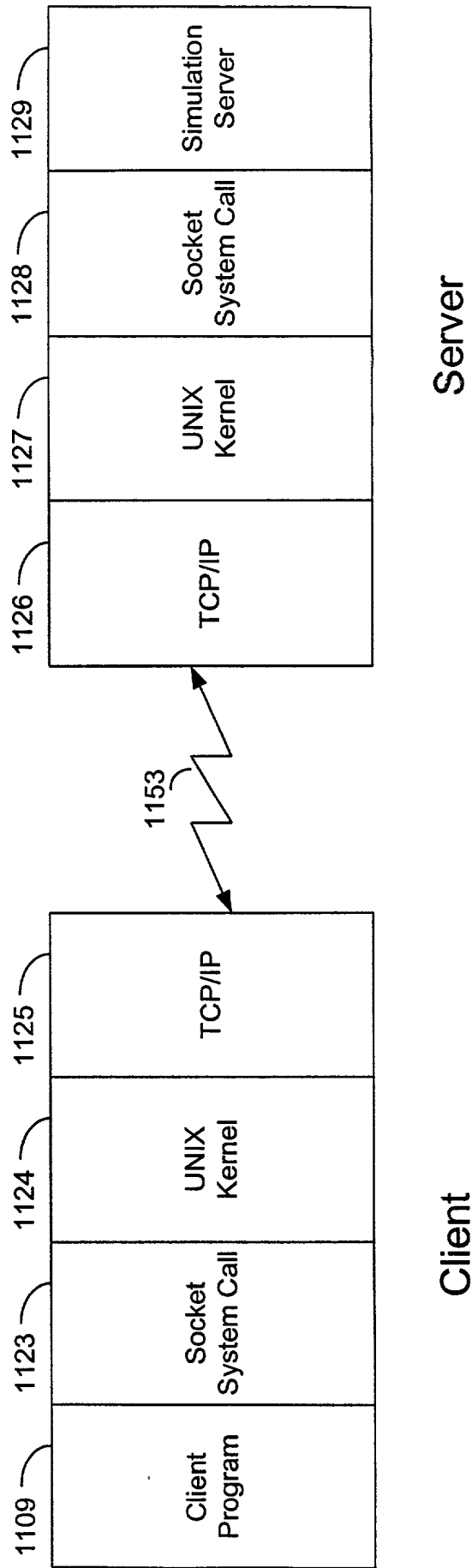


FIG. 55

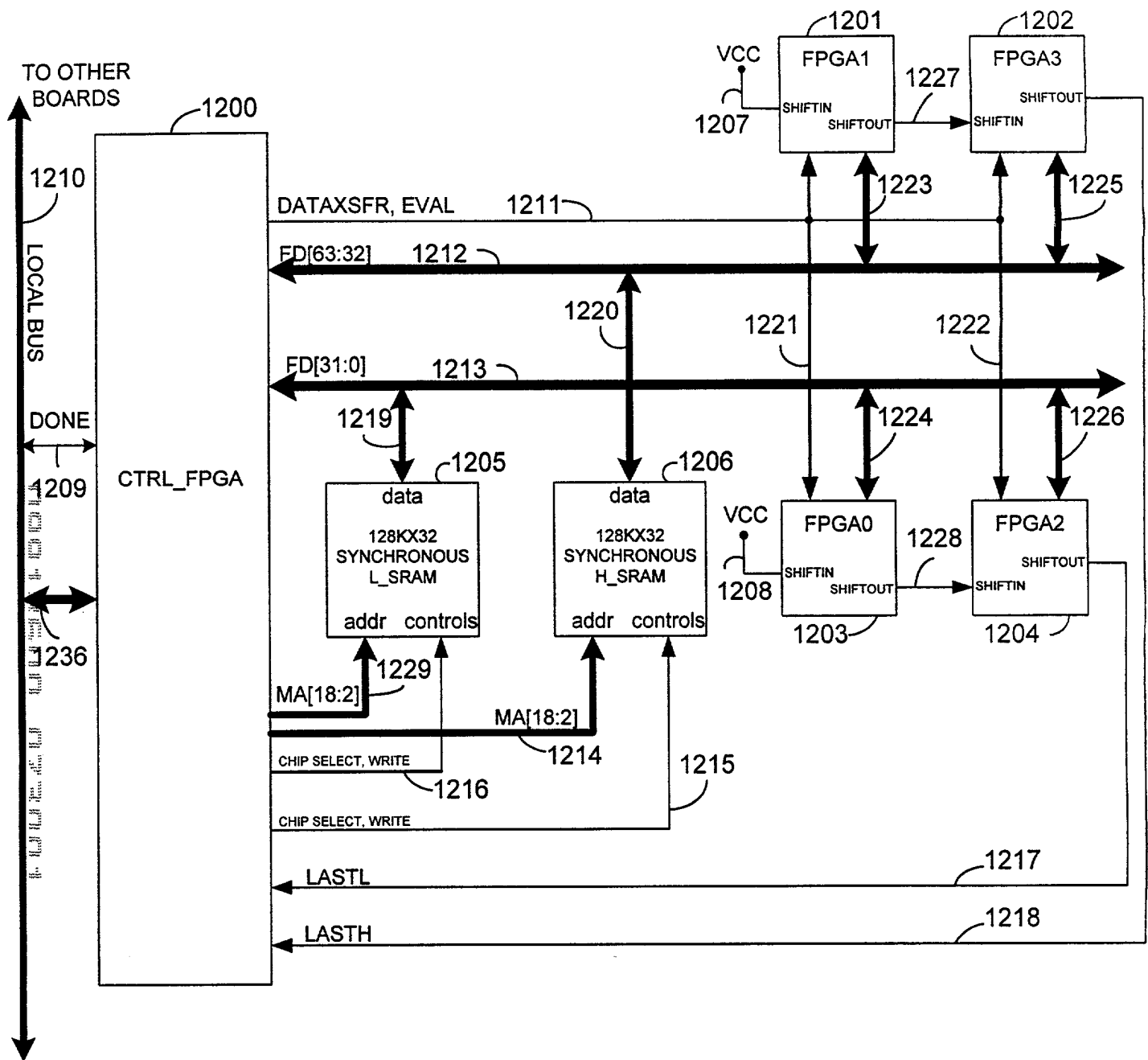
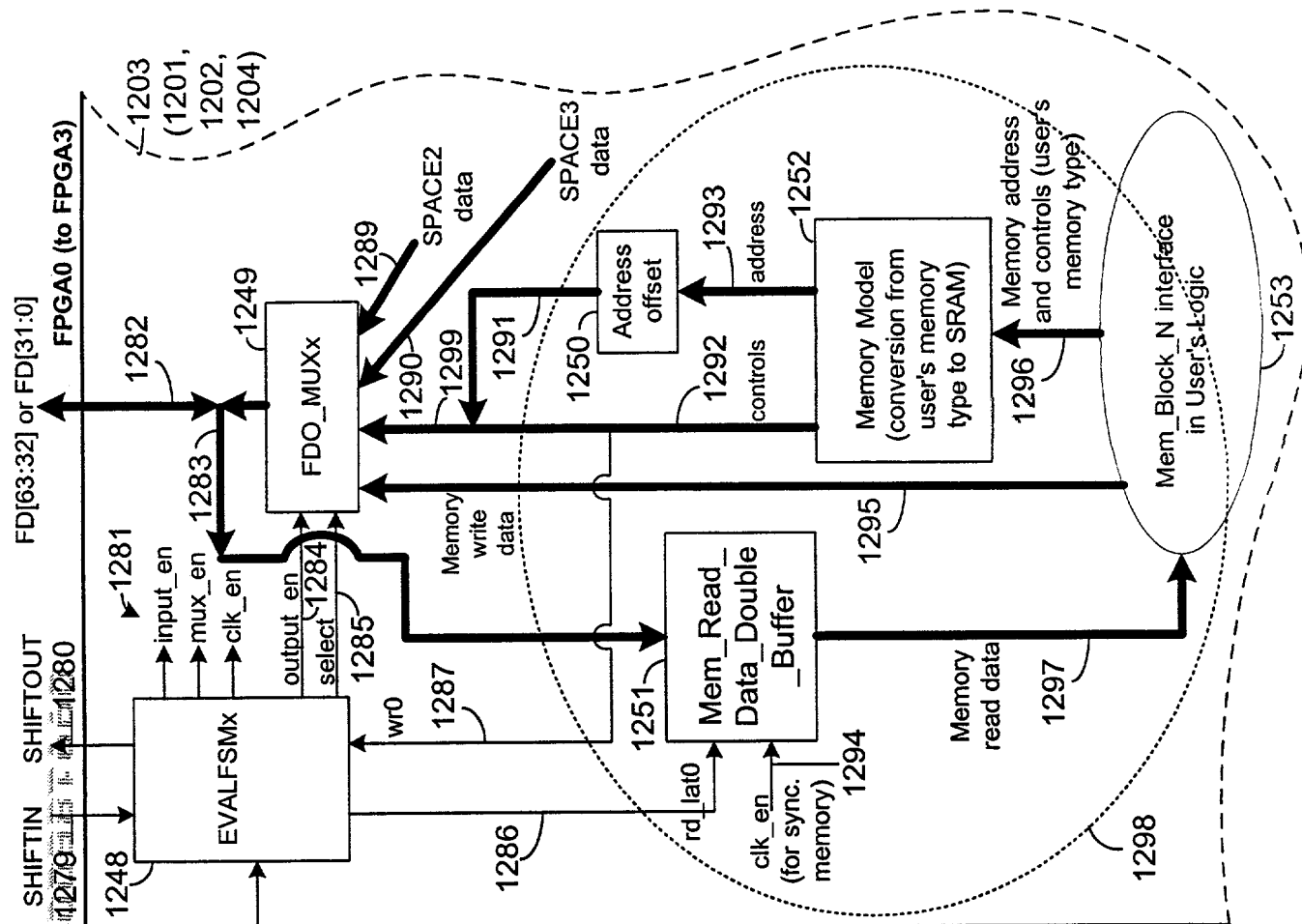


FIG. 56



MEMFSM - Memory Finite State Machine in CTRL_FPGA unit

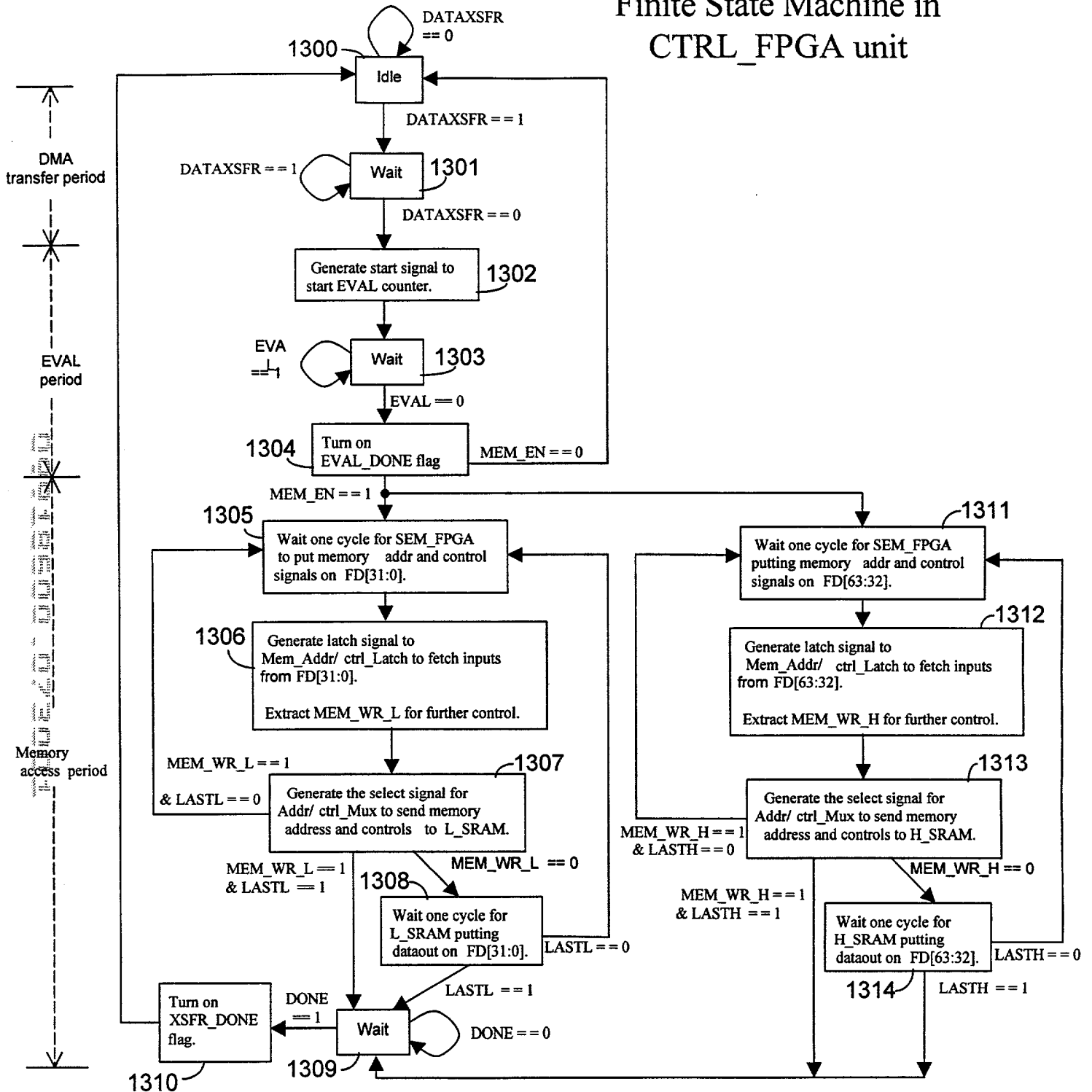


FIG. 58

EVALFSM - EVAL Finite State Machine in each FPGA logic device

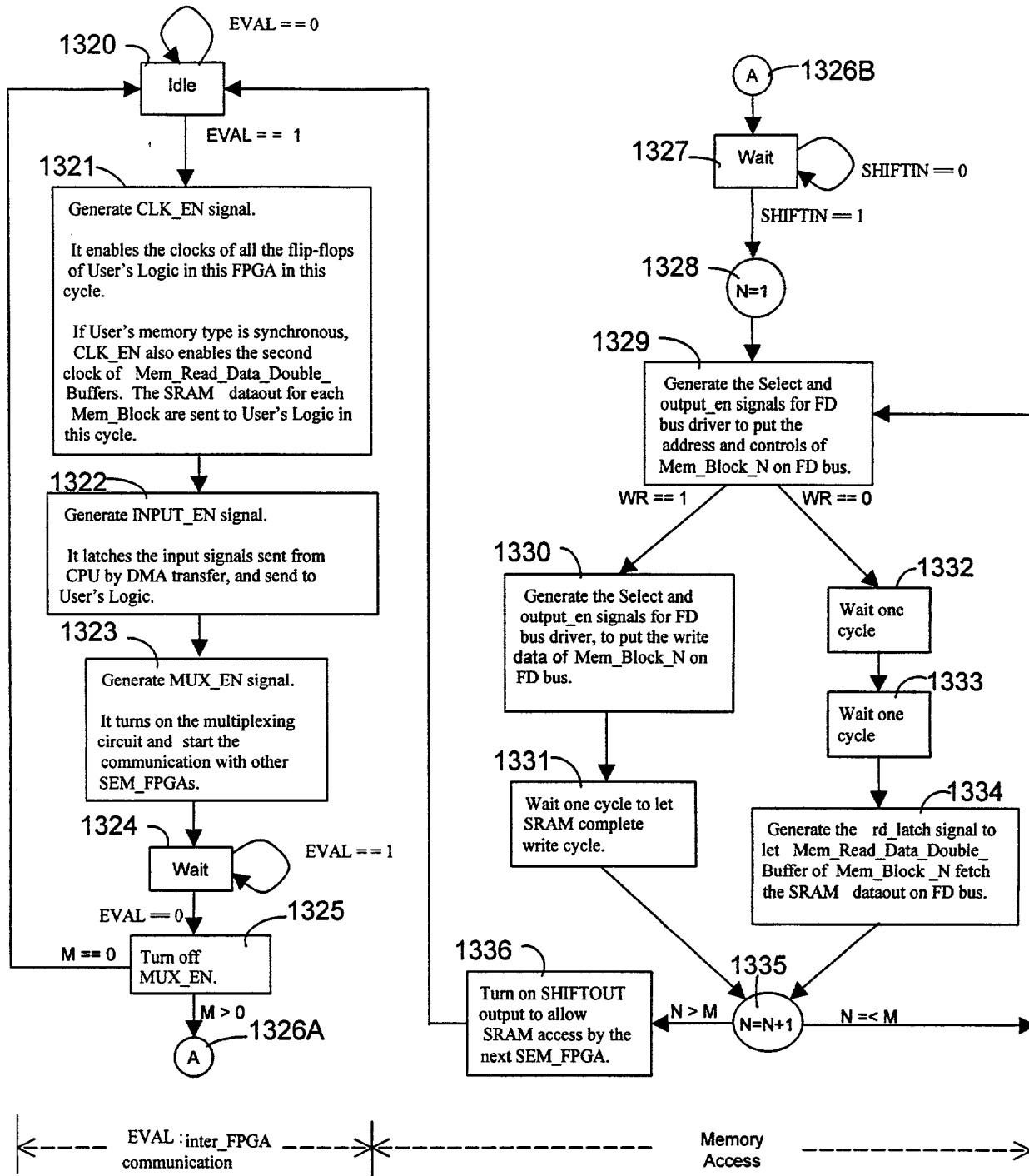


FIG. 59



SIMULATION WRITE/READ CYCLE

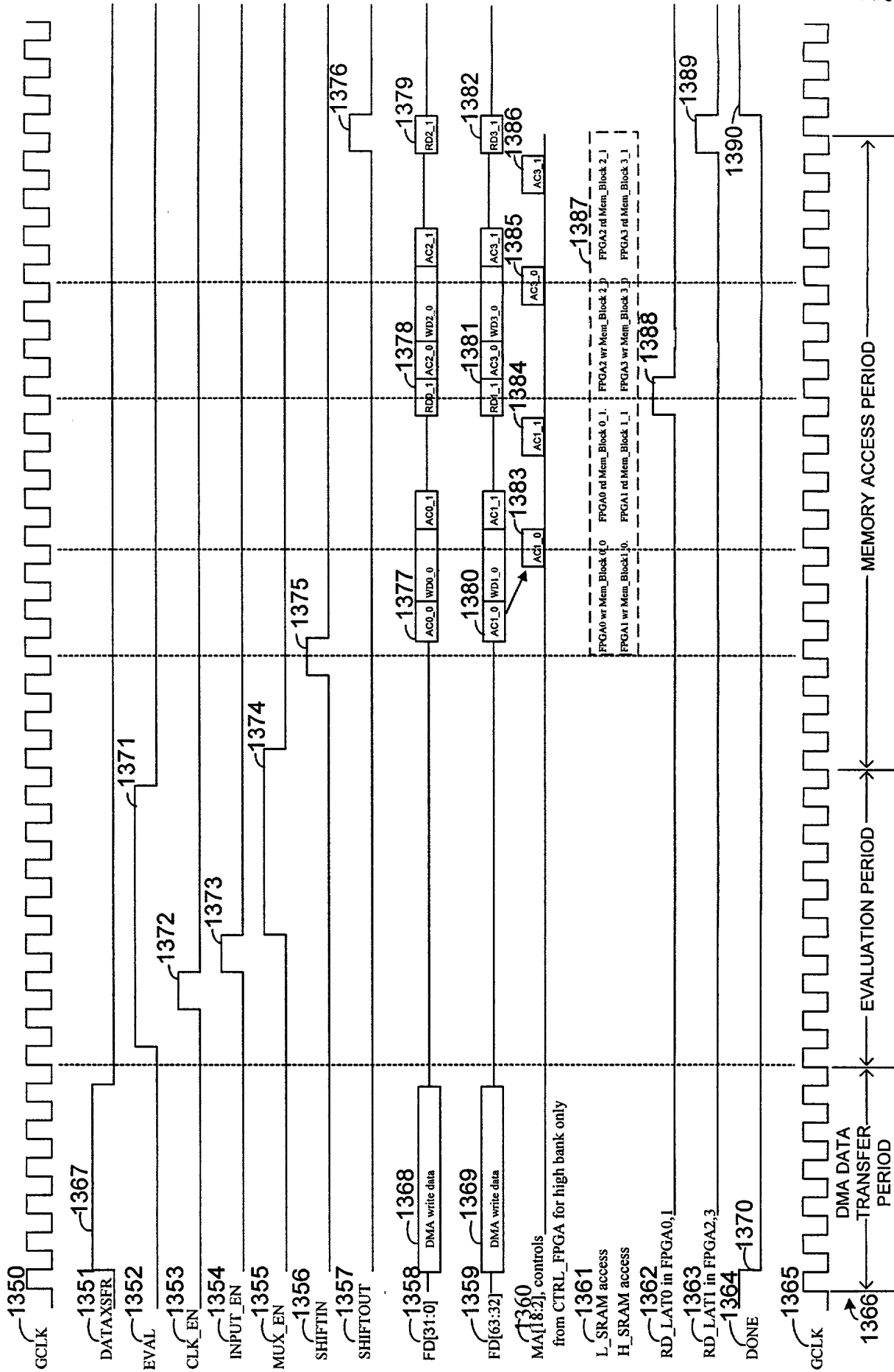


FIG. 61

SIMULATION DATA TRANSFER TIMING

(WR_XSFR_EN=RD_XSFR_EN=1, WAIT_EVAL=0)

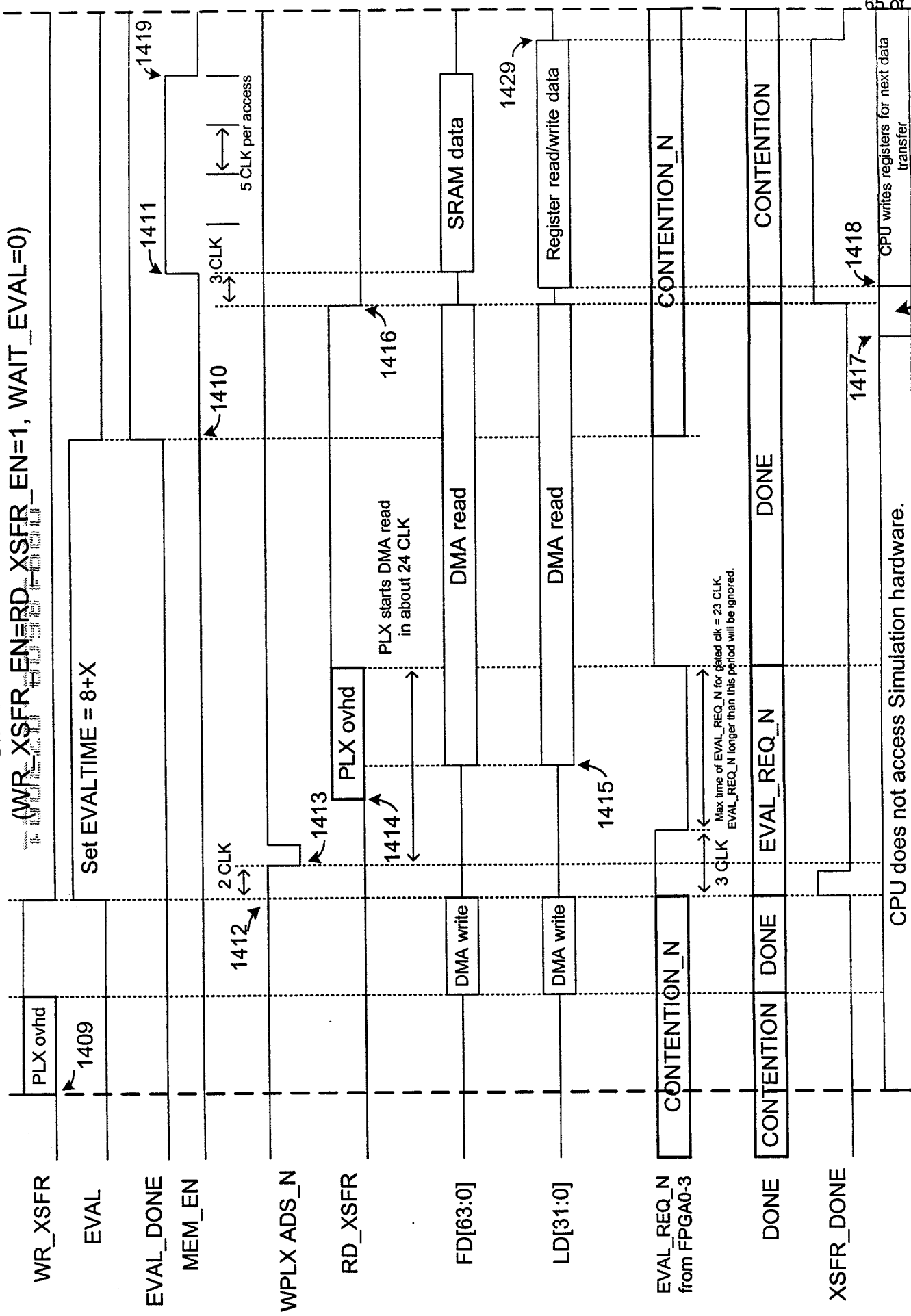


FIG. 62

SIMULATION DATA TRANSFER TIMING

(WR_XSFR_EN=RD_XSFR_EN=1, WAIT_EVAL=1)

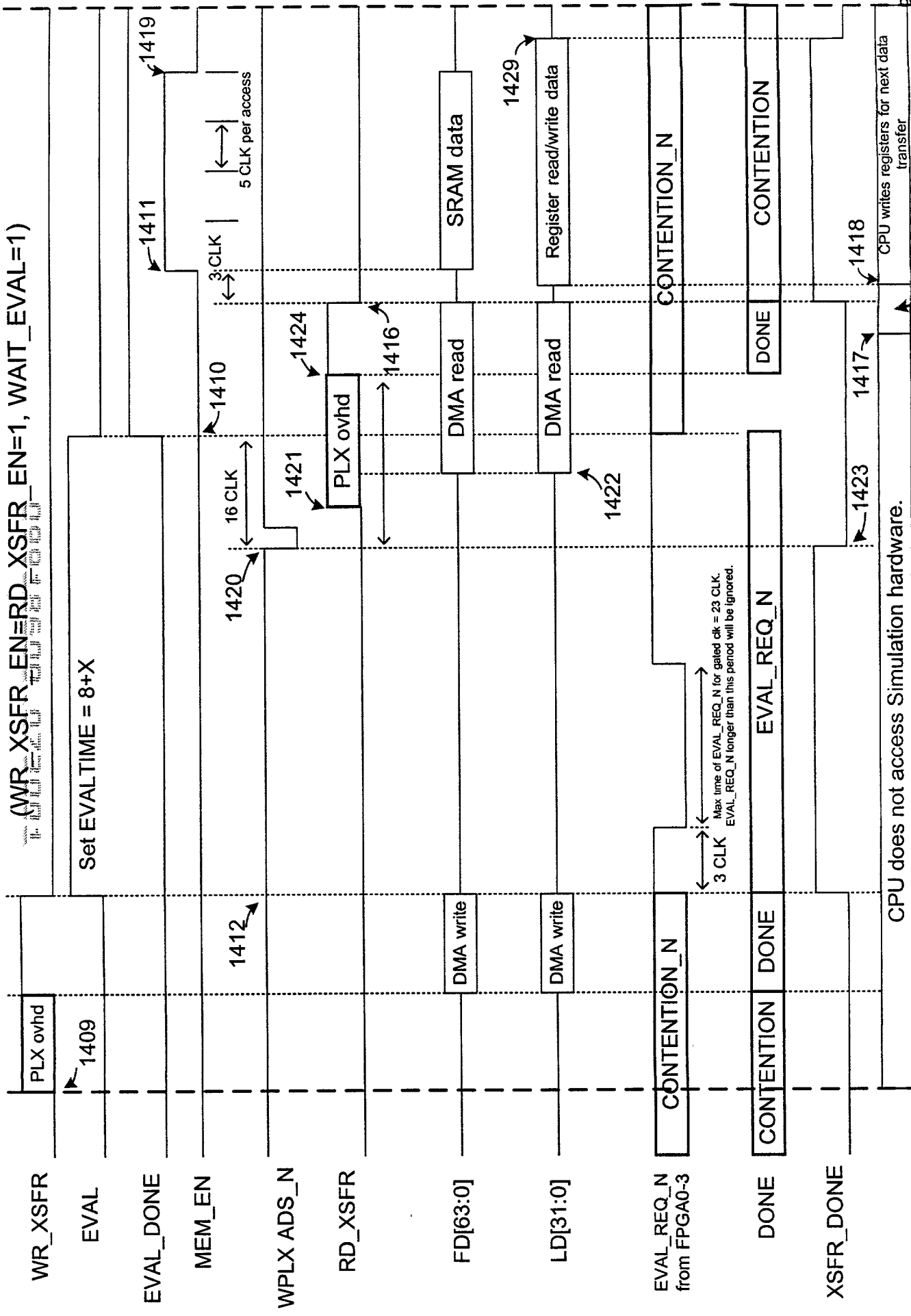


FIG. 63

Typical User Design of PCI Add-on Cards

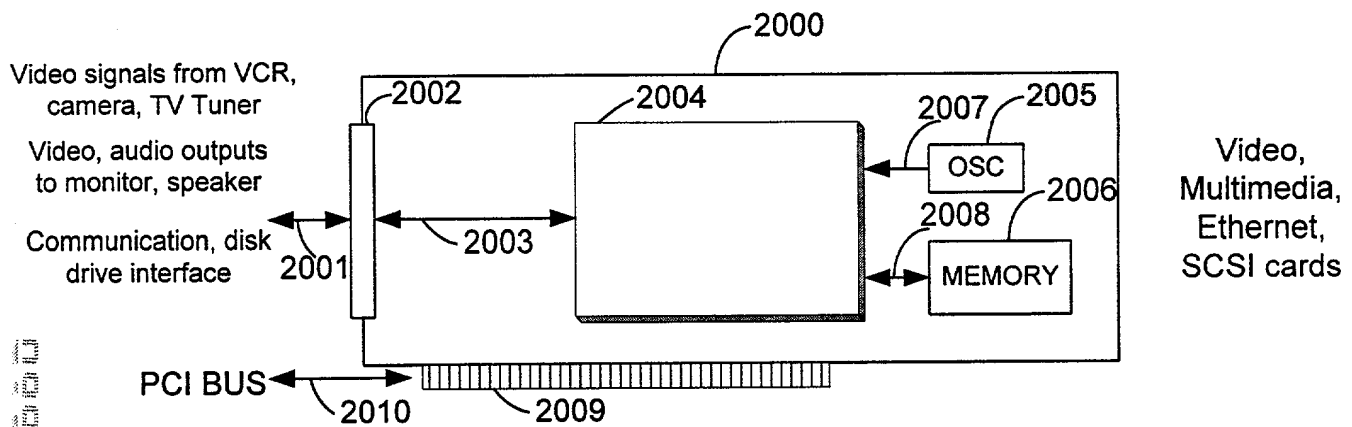


FIG. 64

Typical Hardware/Software Co-Verification

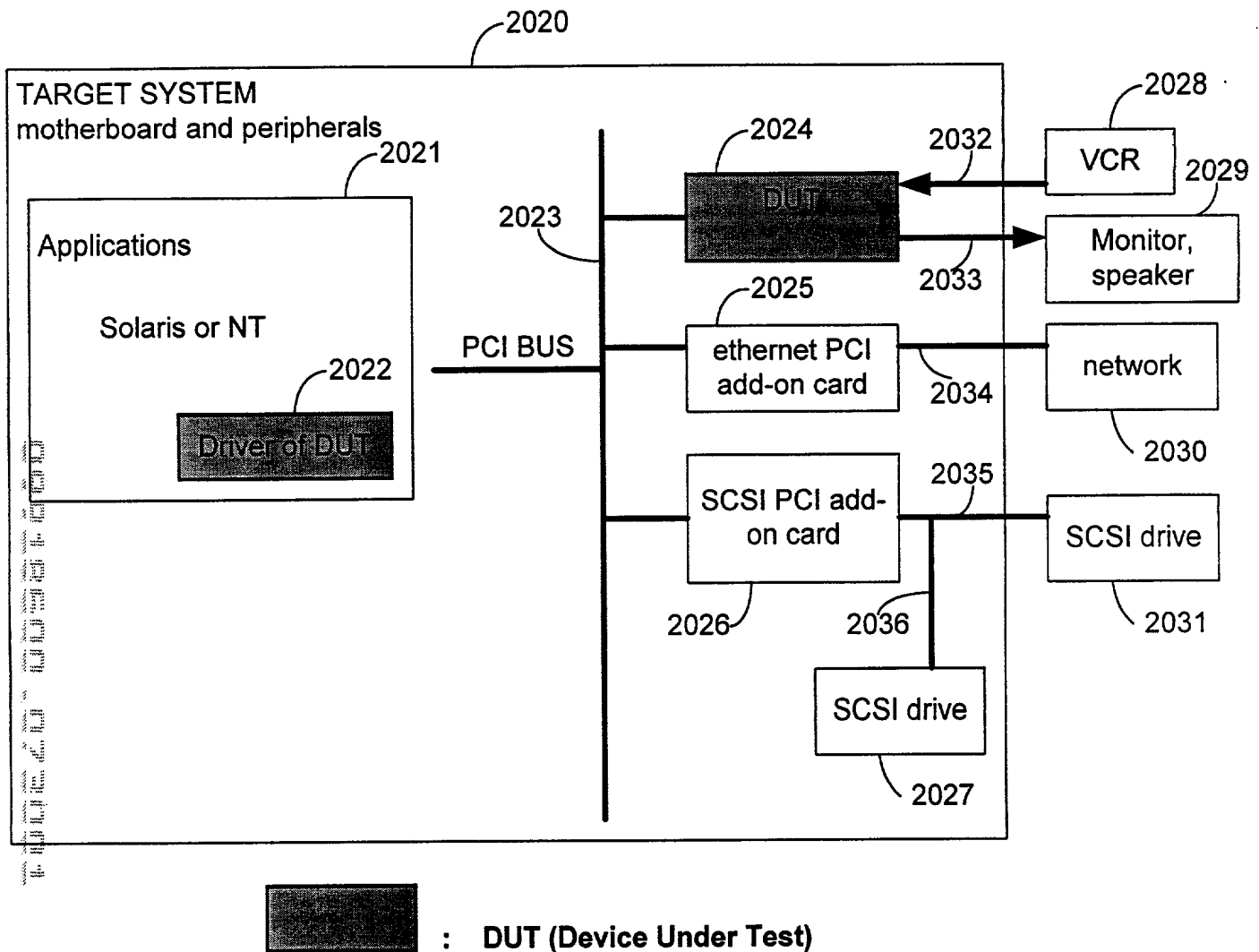
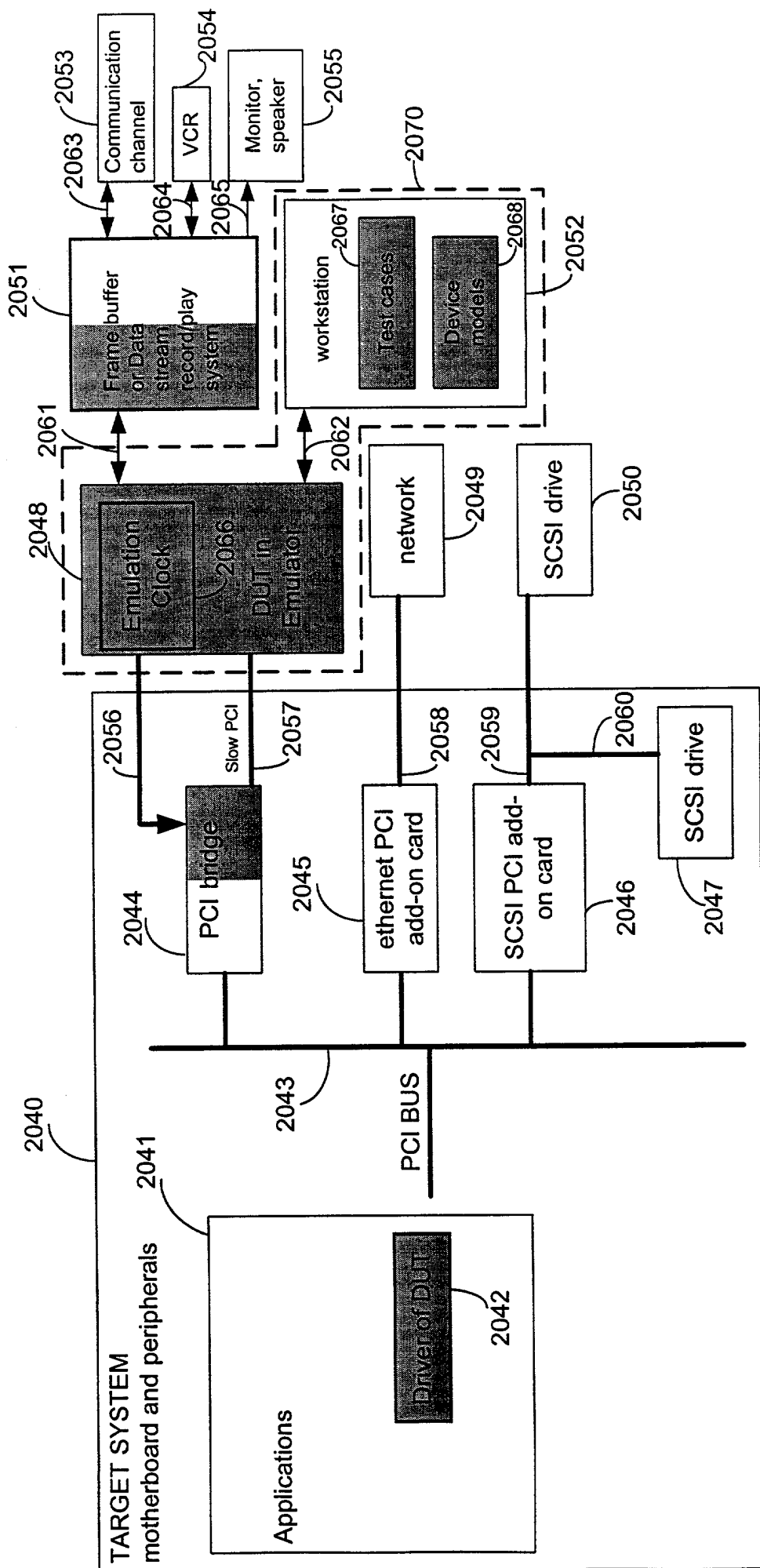


FIG. 65

Typical Co-Verification by Using Emulator




 : running time at emulation speed
The rest of the target system is running at full speed.

FIG. 66

SIMULATION

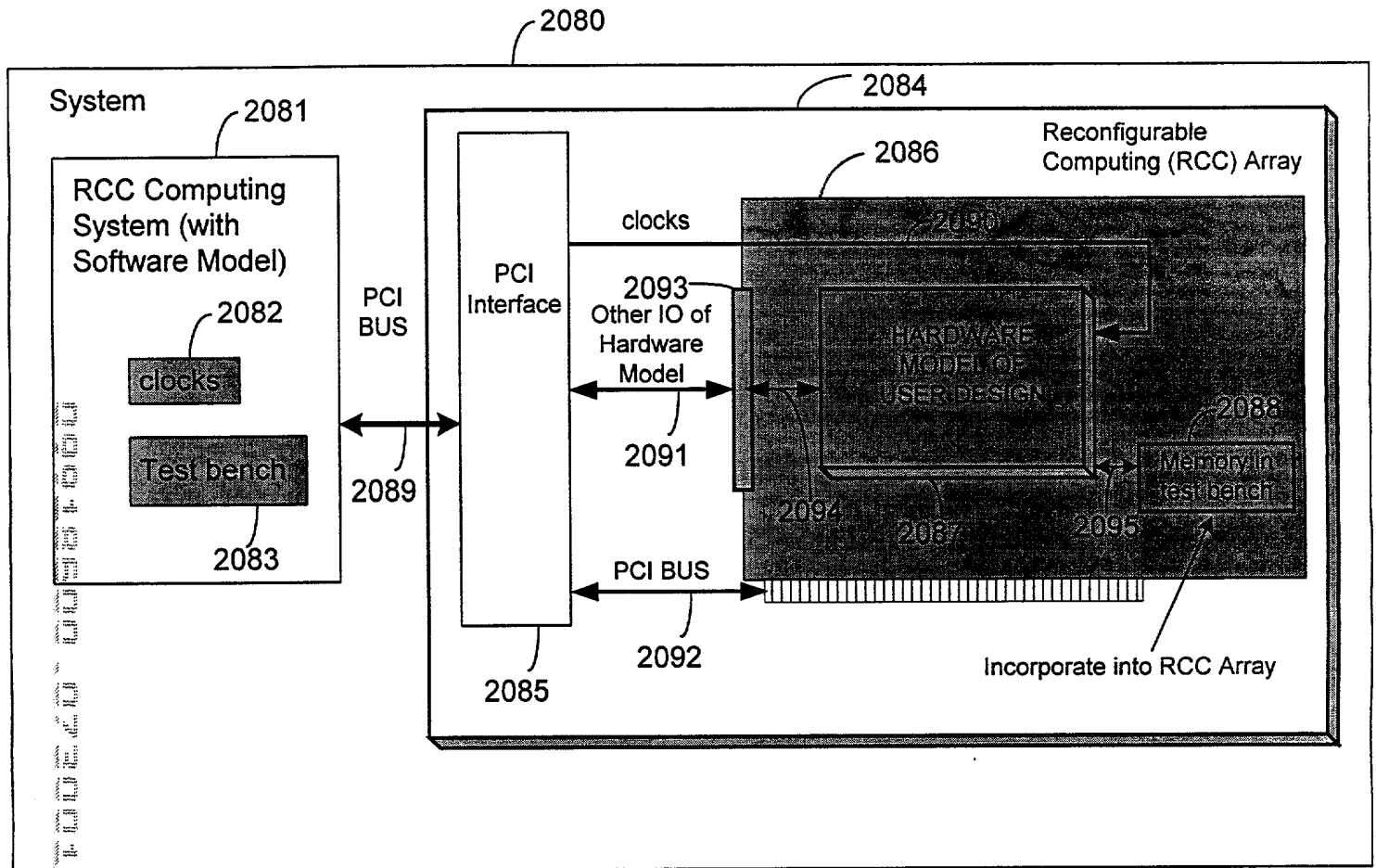


FIG. 67

CO-VERIFICATION WITHOUT EXTERNAL I/O

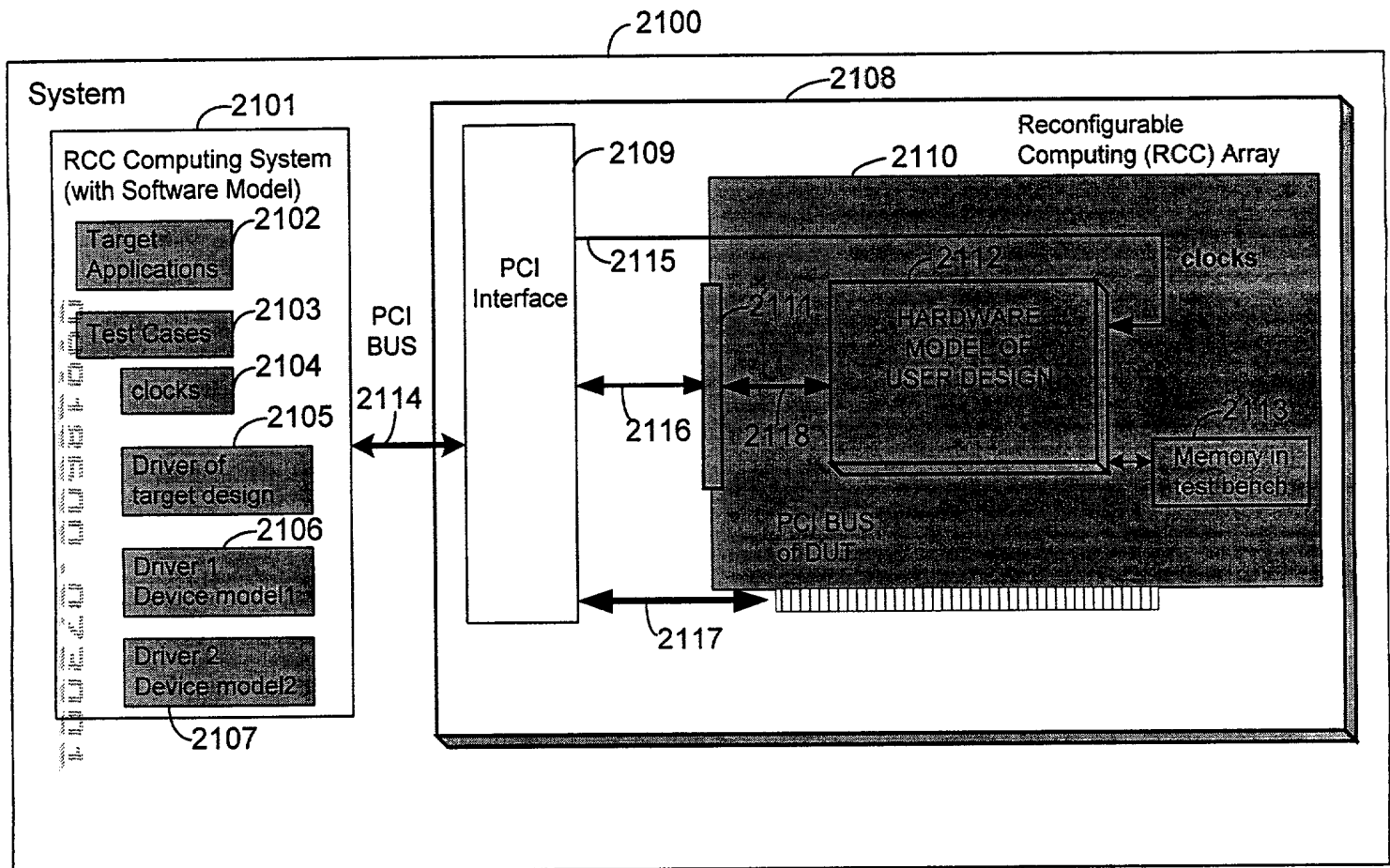


FIG. 68

CO-VERIFICATION WITH EXTERNAL I/O

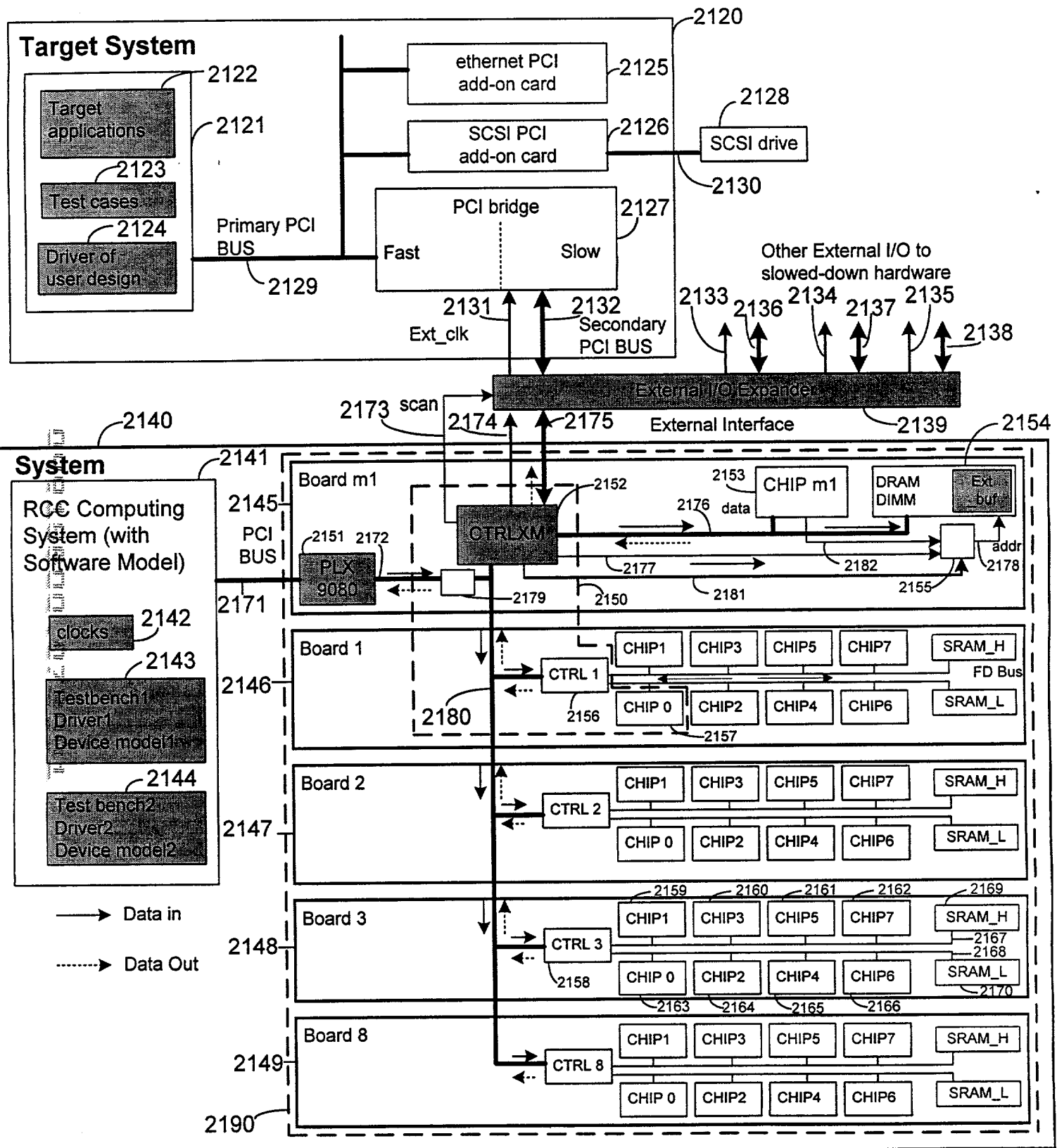


FIG. 69

CONTROL OF DATA-IN CYCLE

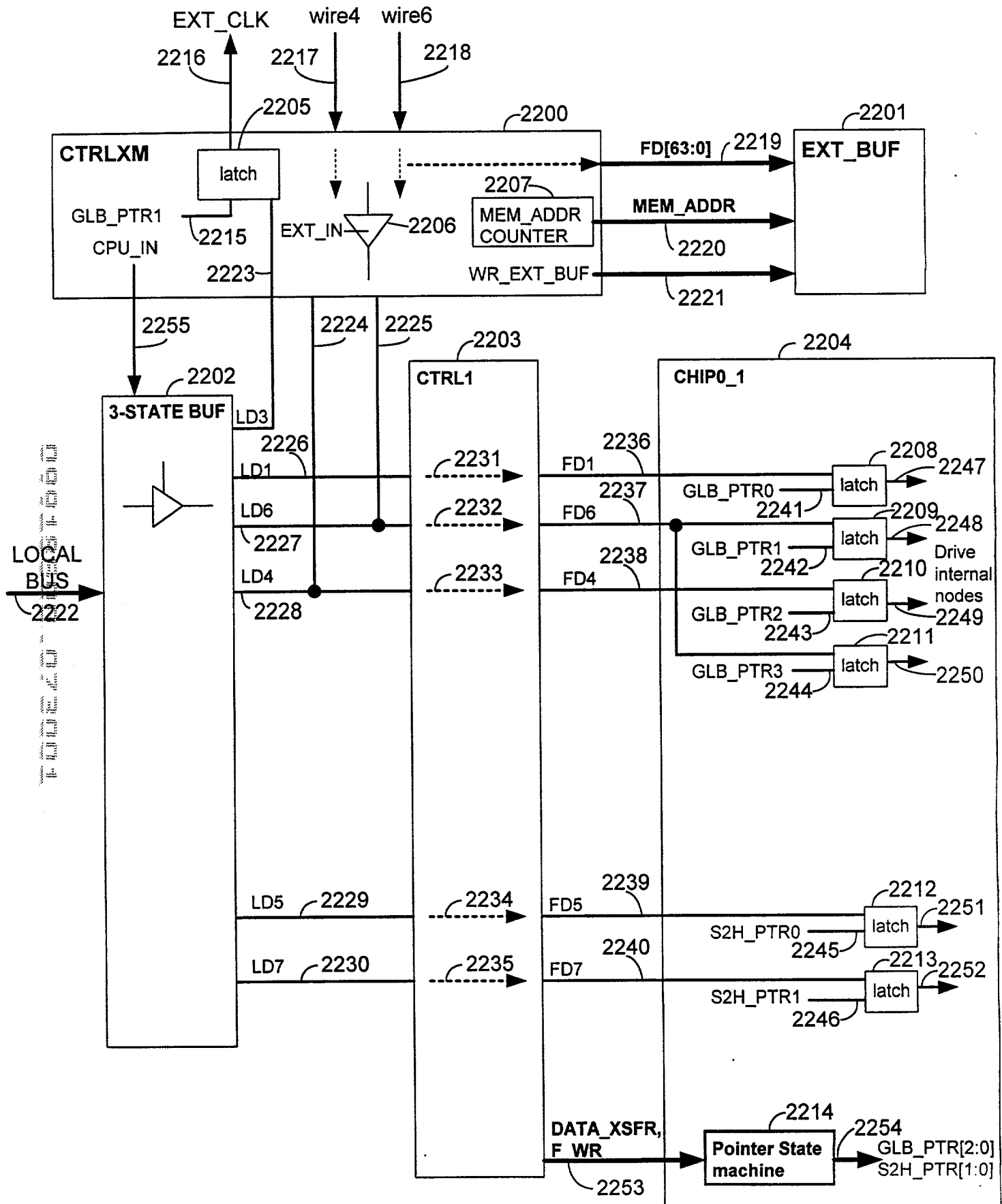


FIG. 70

CONTROL OF DATA-OUT CYCLE

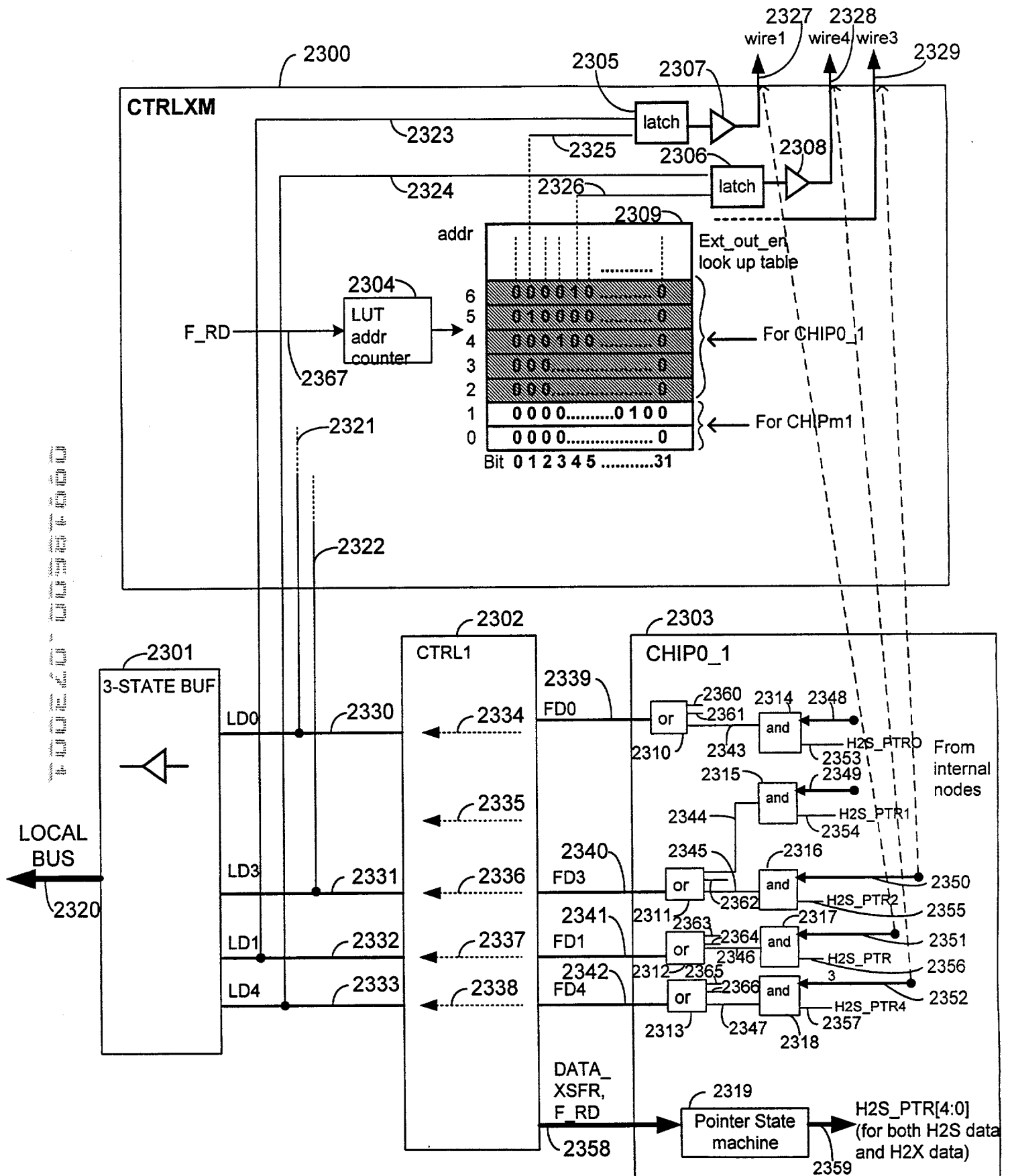


FIG. 71

CONTROL OF DATA-IN CYCLE

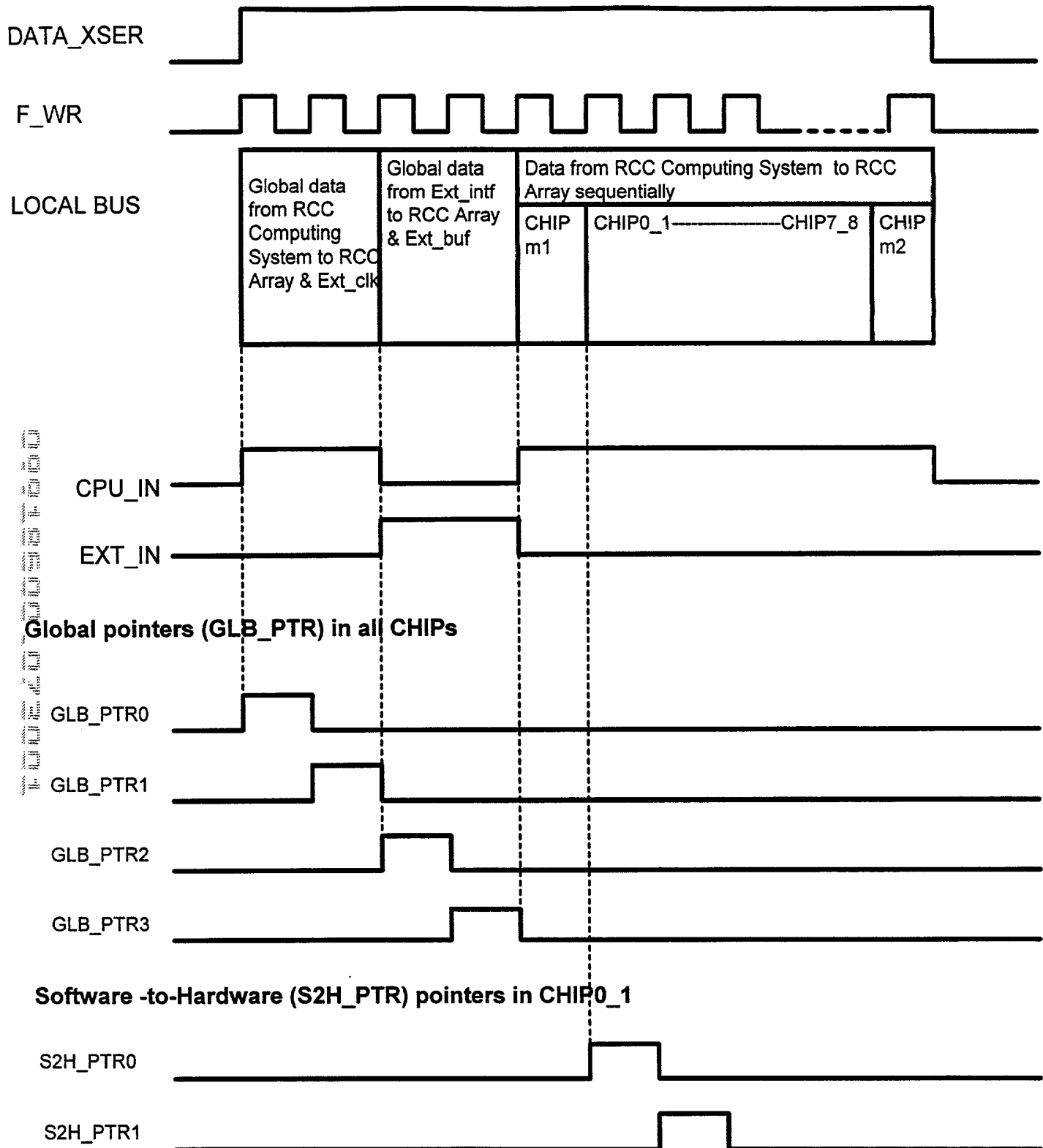


FIG. 72

CONTROL OF DATA-OUT CYCLE

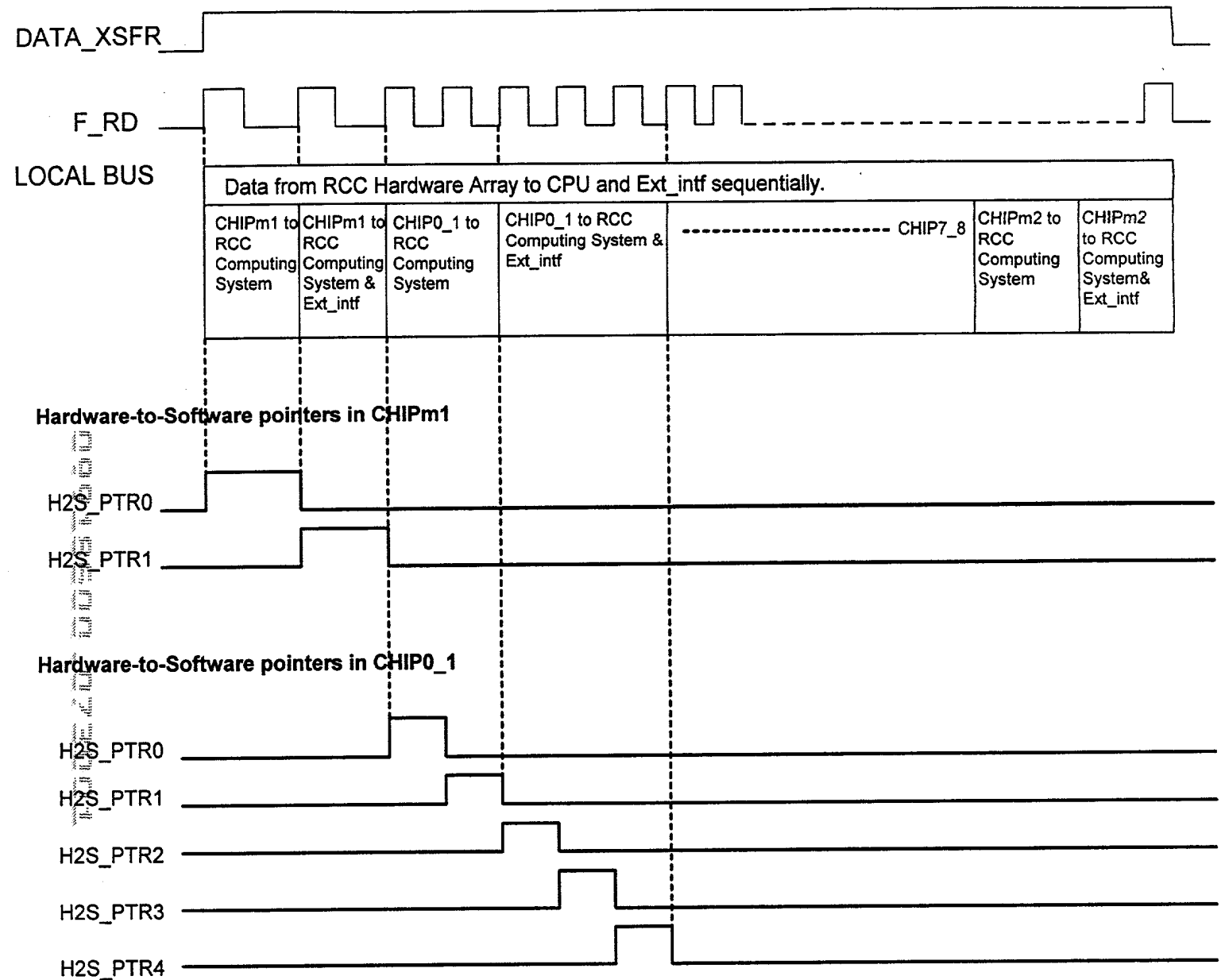


FIG. 73

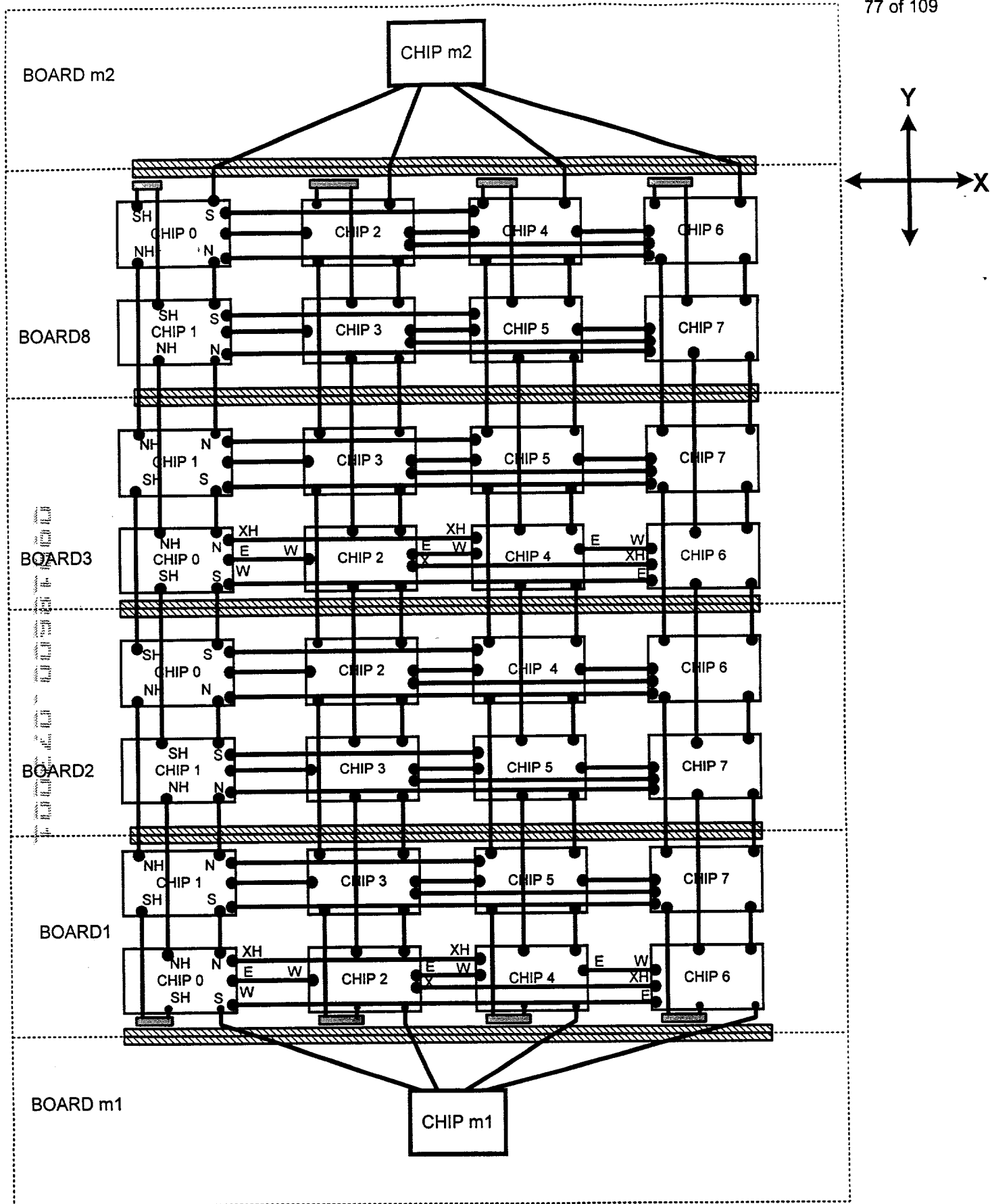


FIG. 74

SHIFT REGISTER

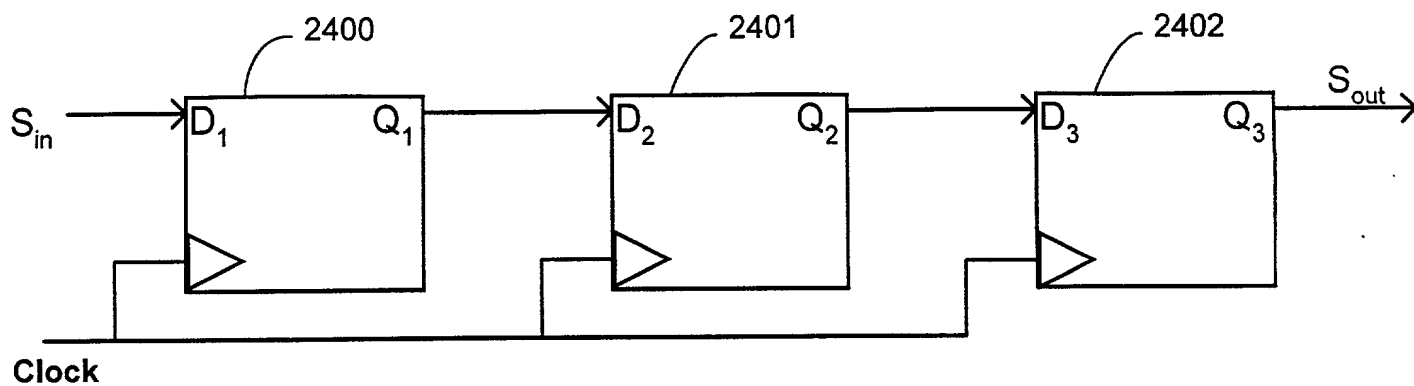


FIG. 75(A)

HOLD TIME ASSUMPTION FOR SHIFT REGISTER

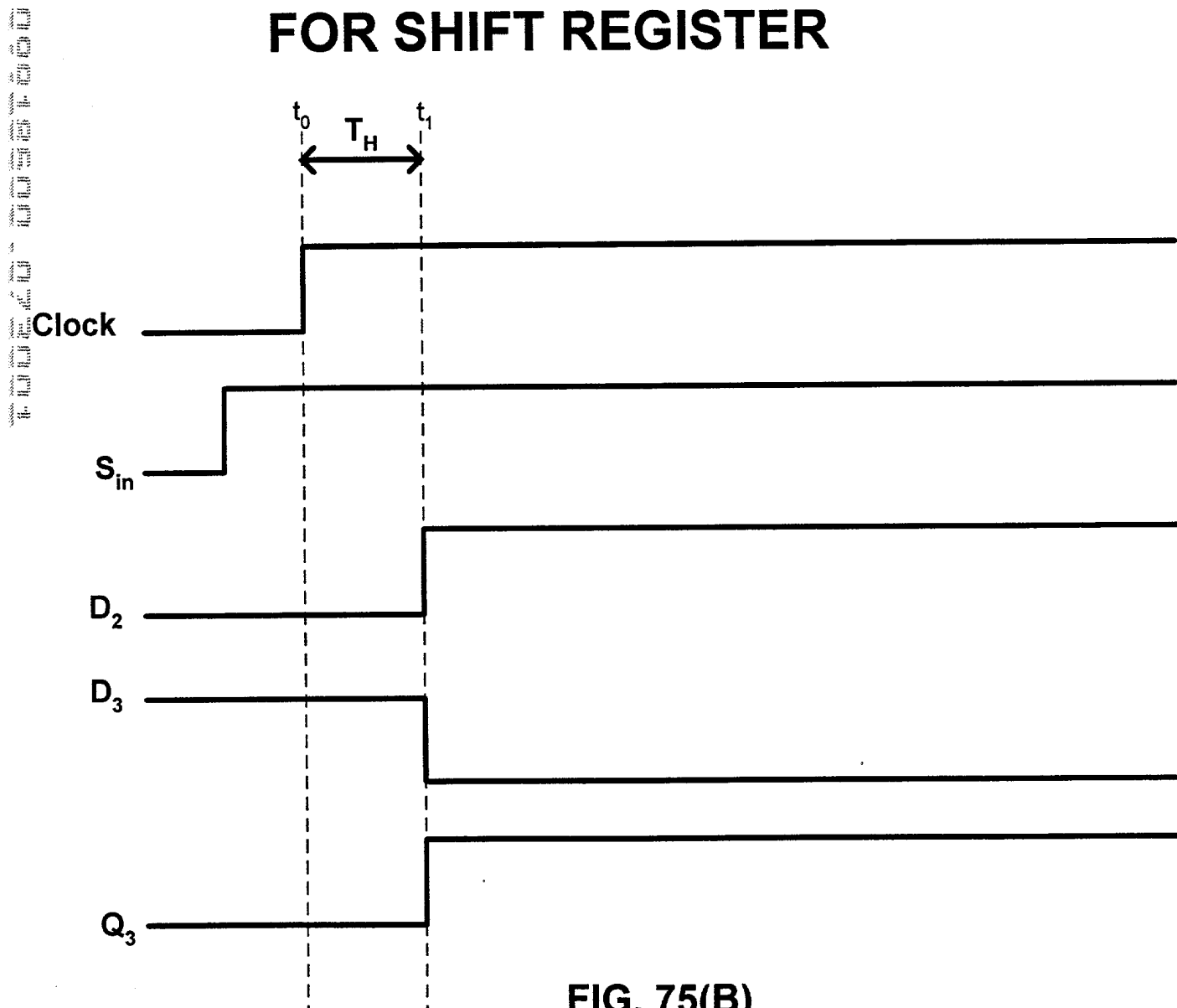
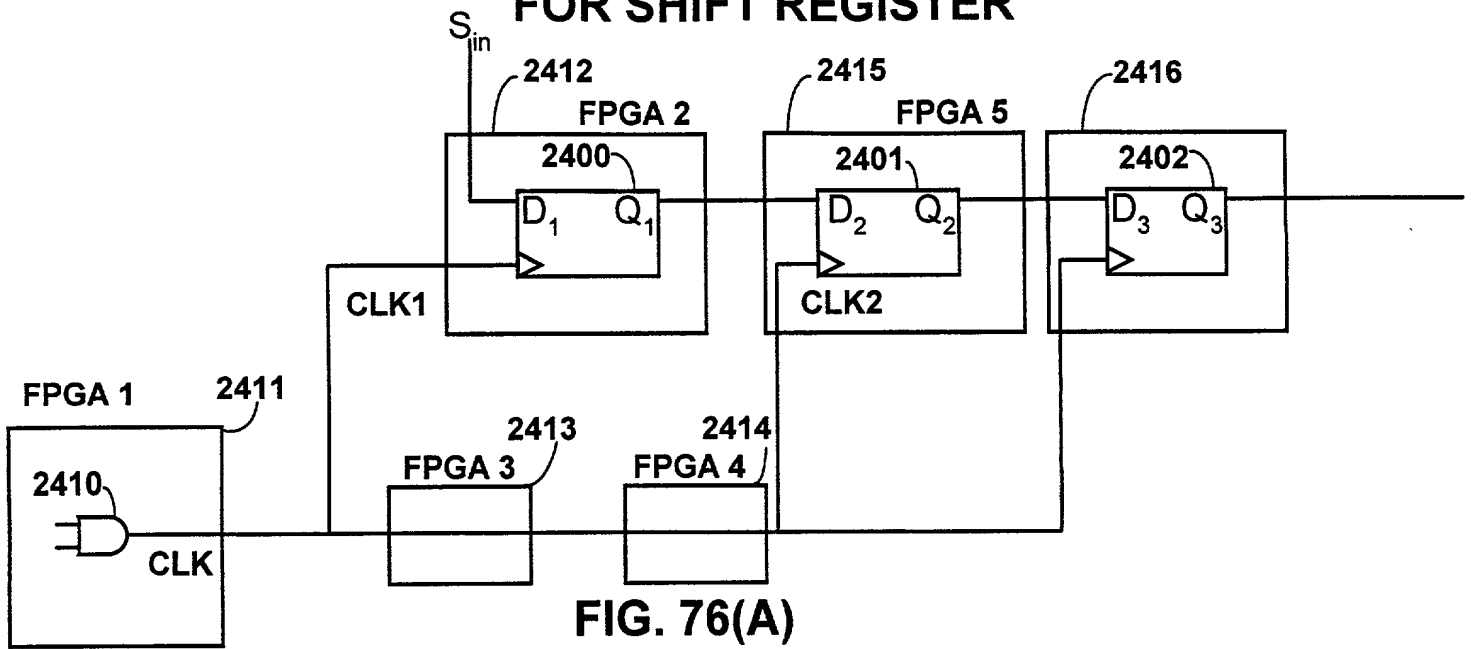
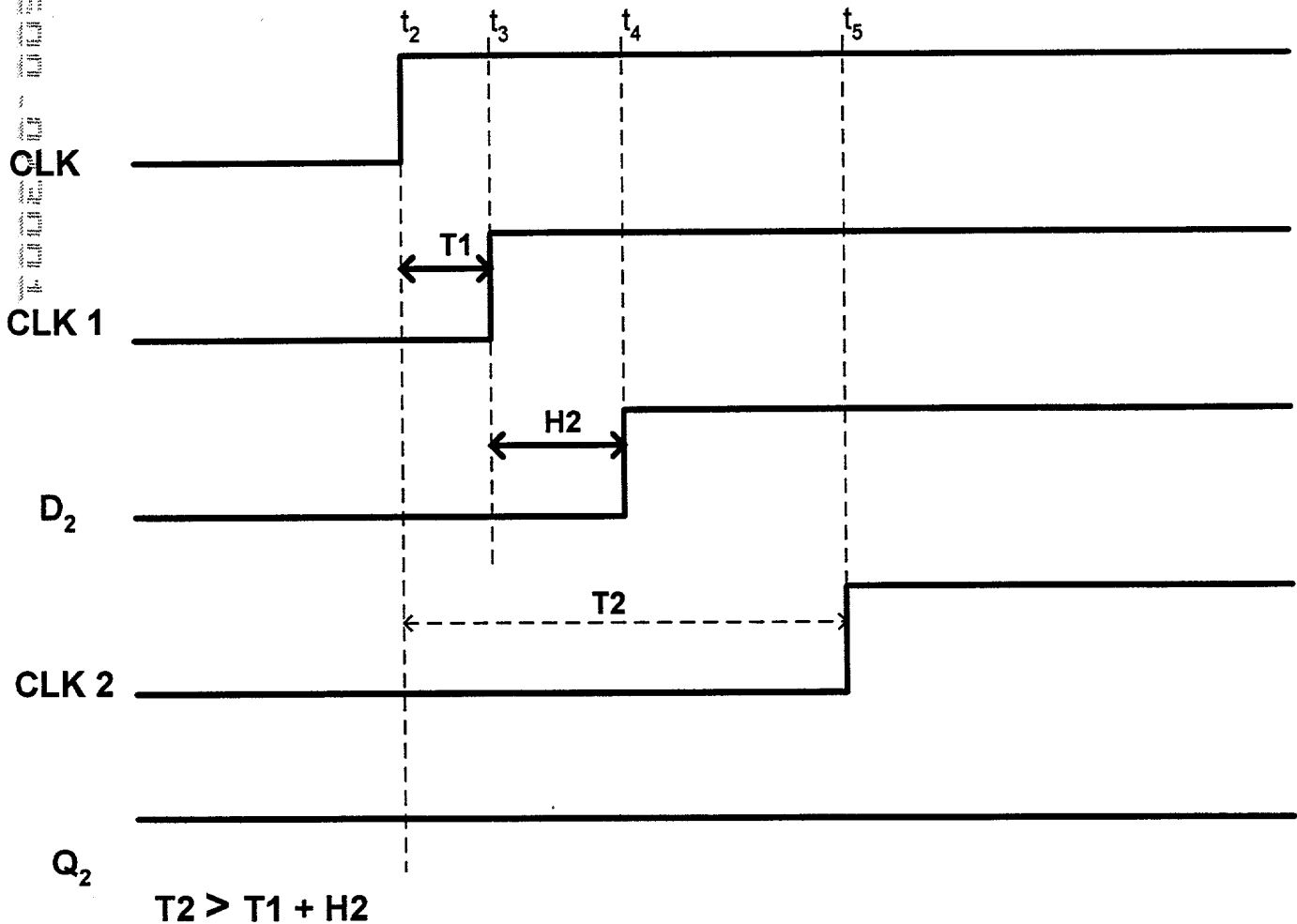


FIG. 75(B)

MULTIPLE FPGA MAPPING FOR SHIFT REGISTER



HOLD TIME VIOLATION BY LONG CLOCK SKEW



CLOCK GLITCH PROBLEM

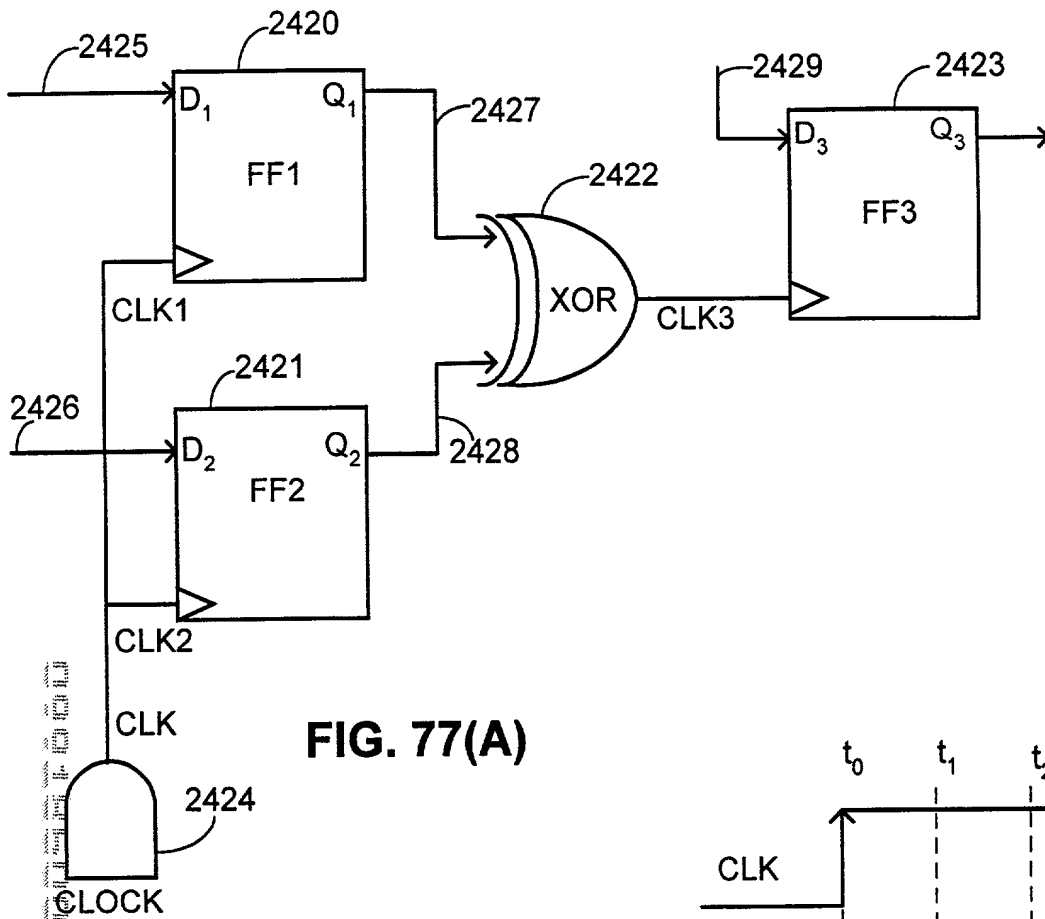


FIG. 77(A)

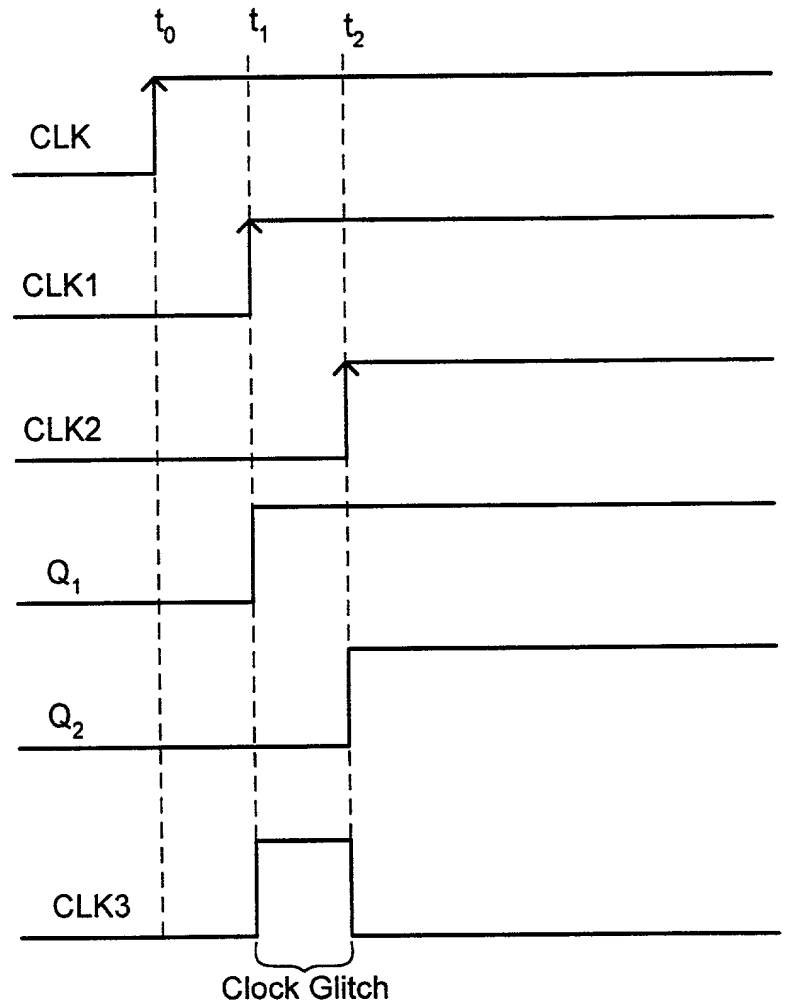
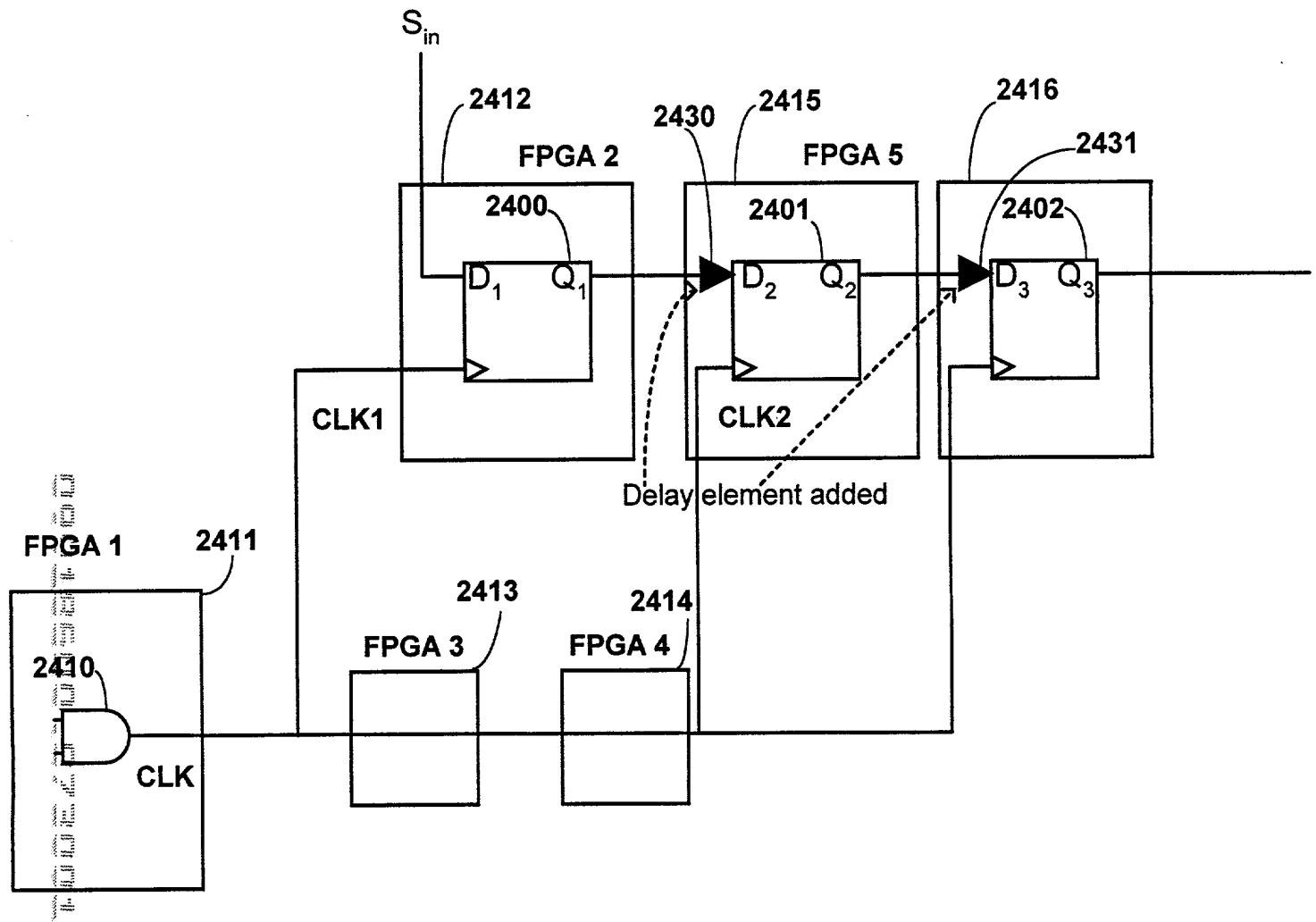


FIG. 77(B)

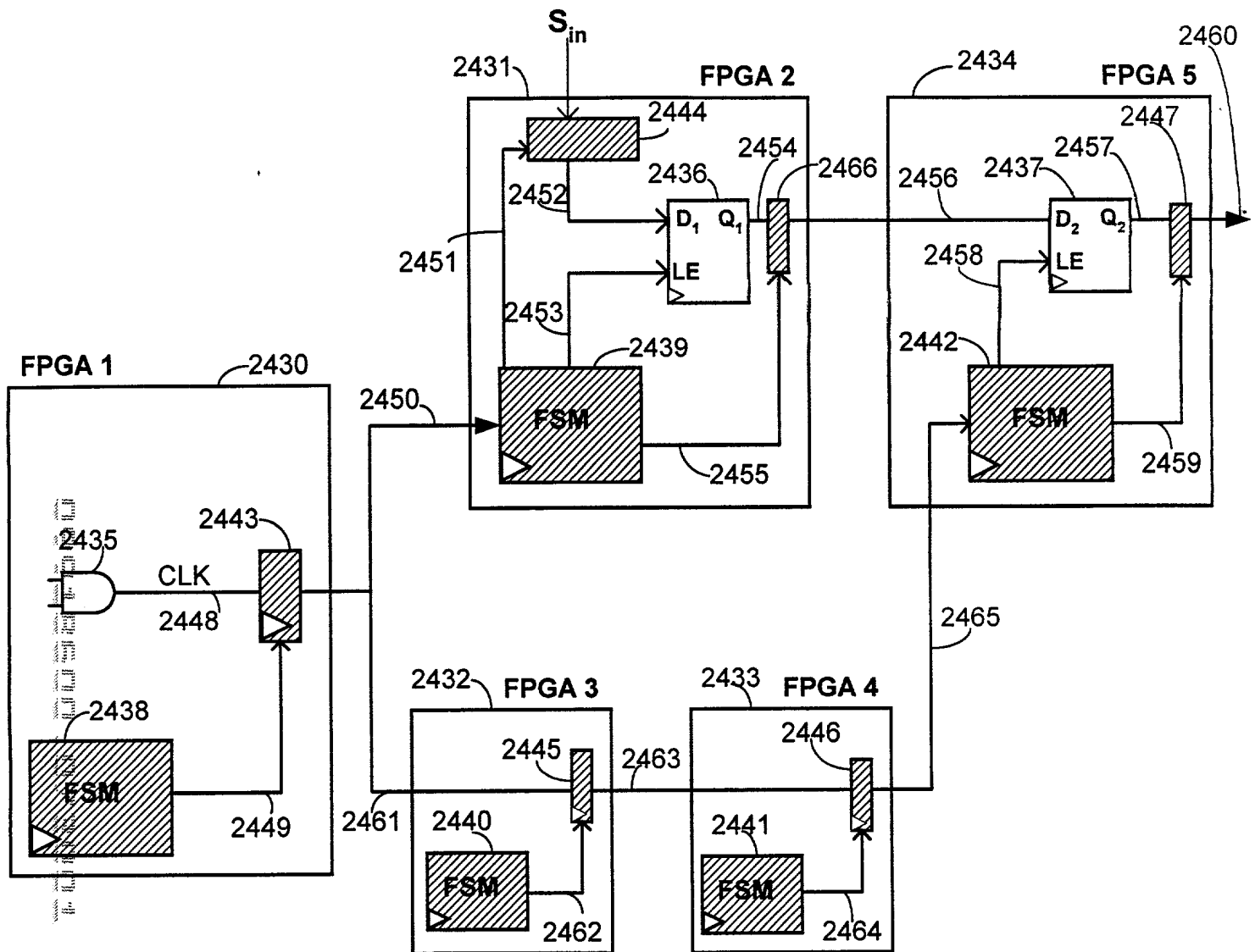
TIMING ADJUSTMENT BY ADDING DELAY



(Prior Art)

FIG. 78

GLOBAL RETIMING



Legend

▷ Controlled by the global reference clock.

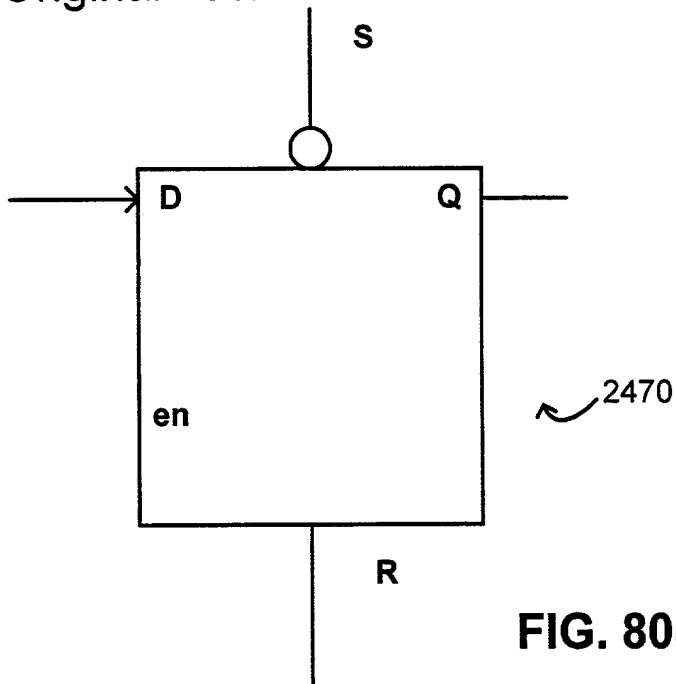
▨ FSM and I/O registers for retiming control.

(Prior Art)

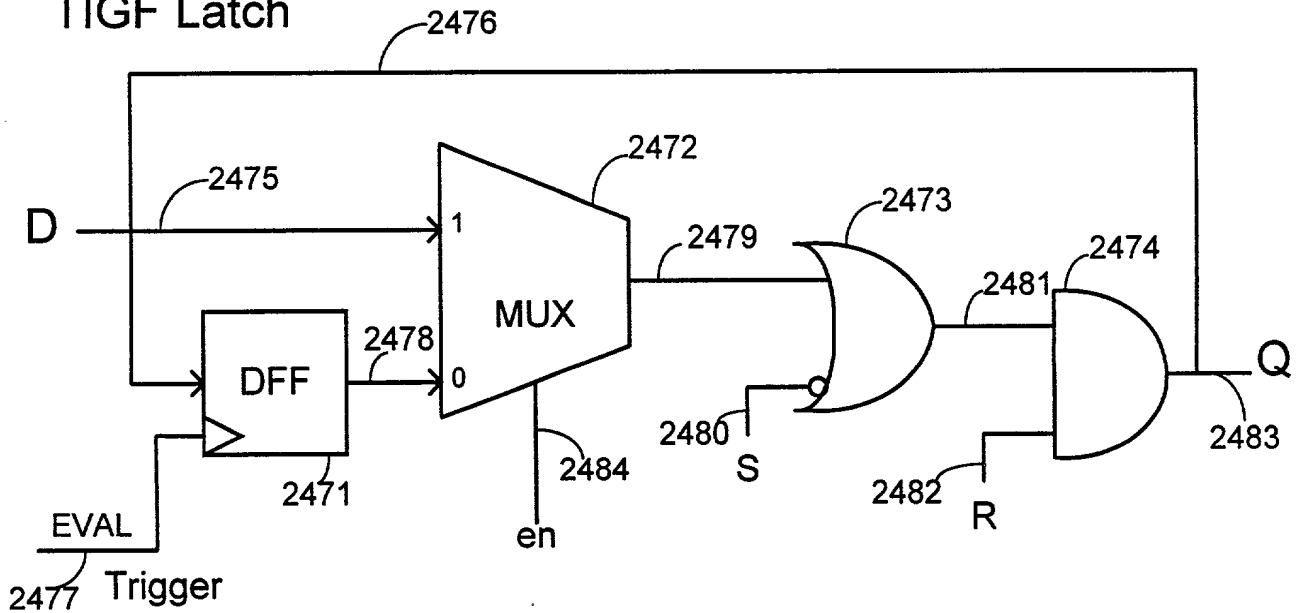
FIG. 79

TIGF LATCH

Original Latch



TIGF Latch



TIGF DFF

Original DFF

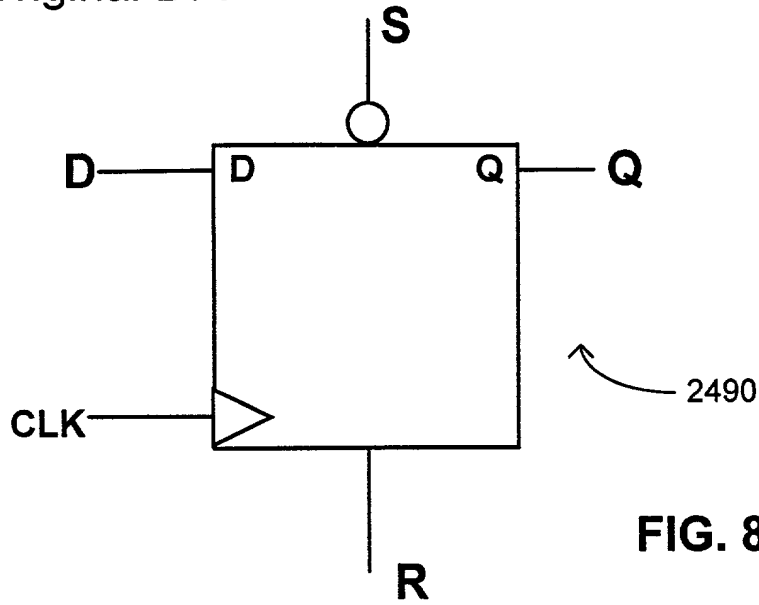


FIG. 81(A)

TIGF DFF and Edge Detector

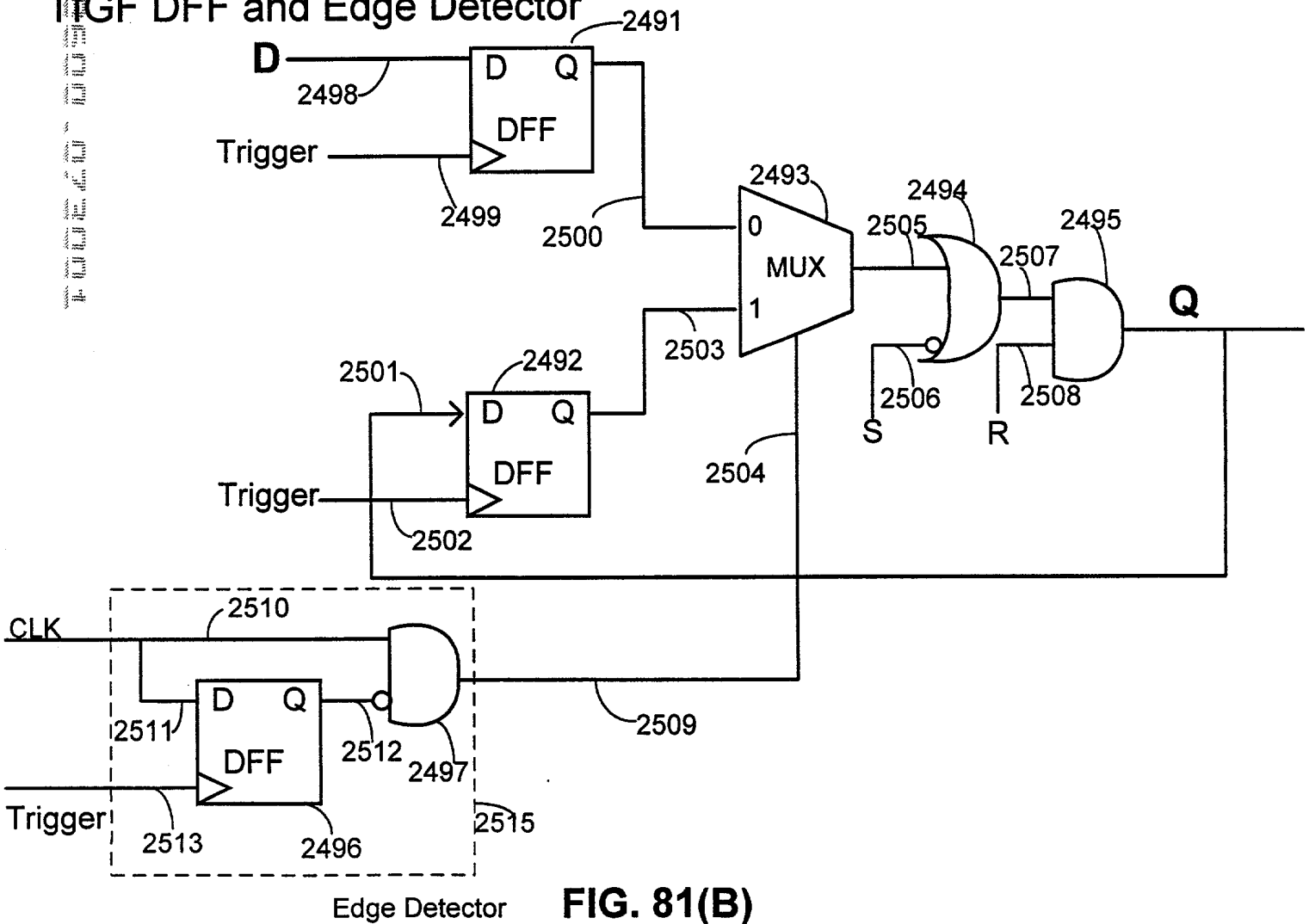


FIG. 81(B)

GLOBAL TRIGGER SIGNAL

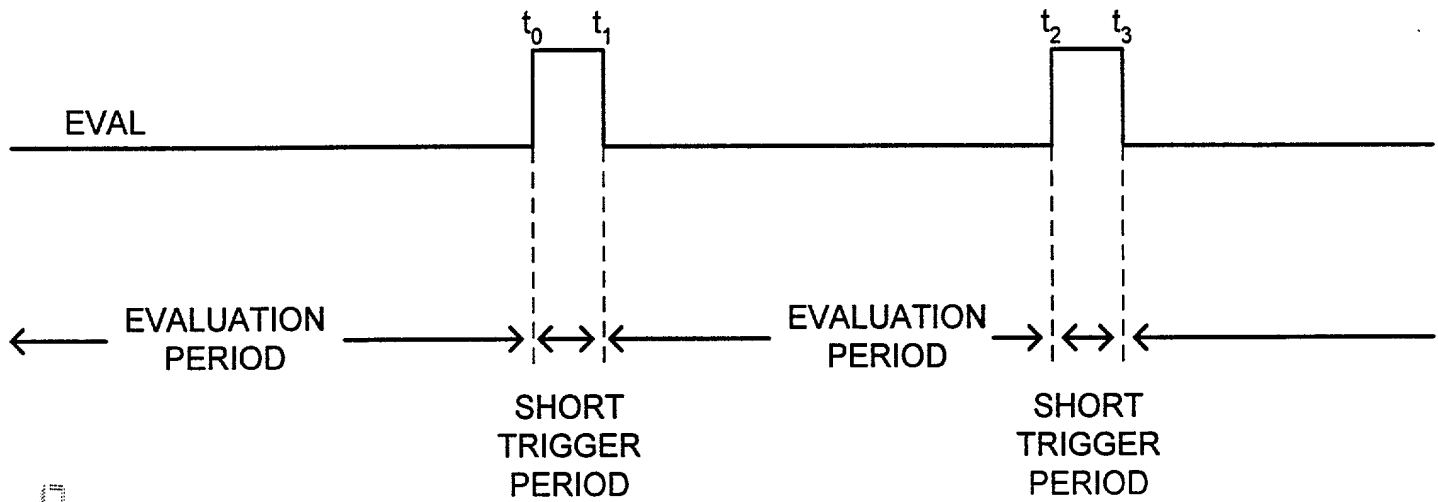


FIG. 82

RCC System

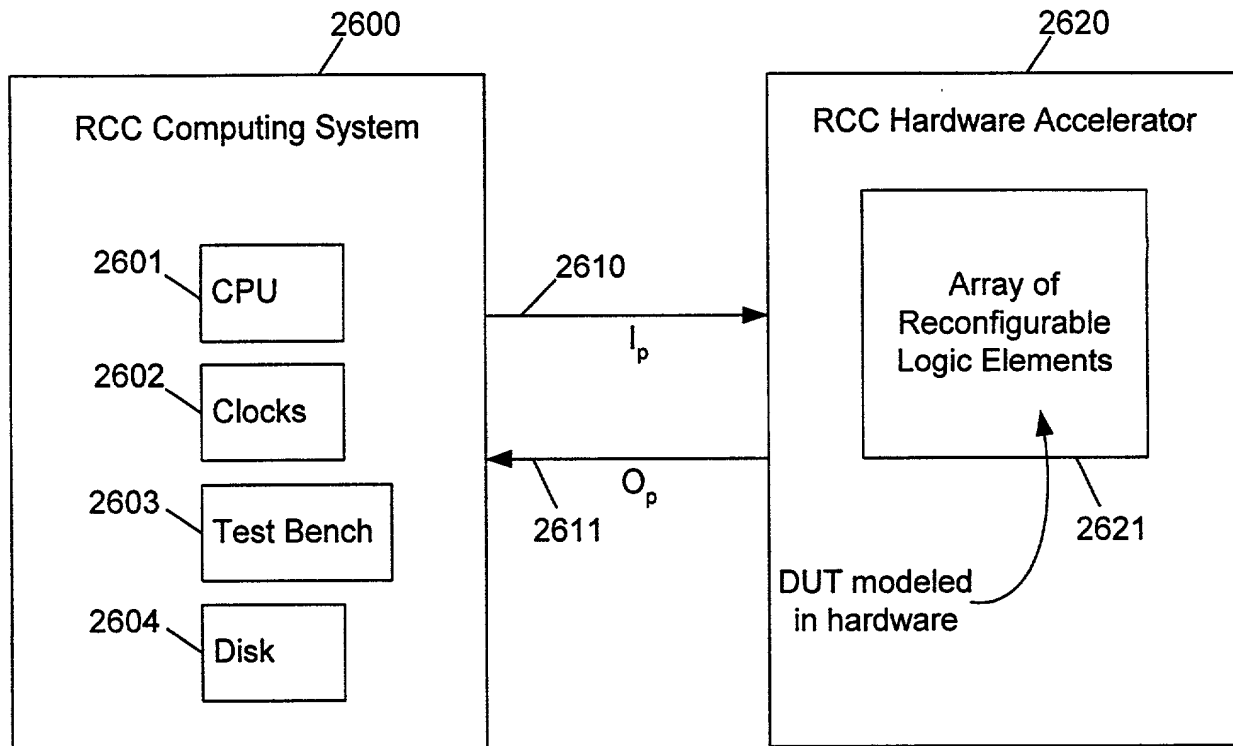


FIG. 83

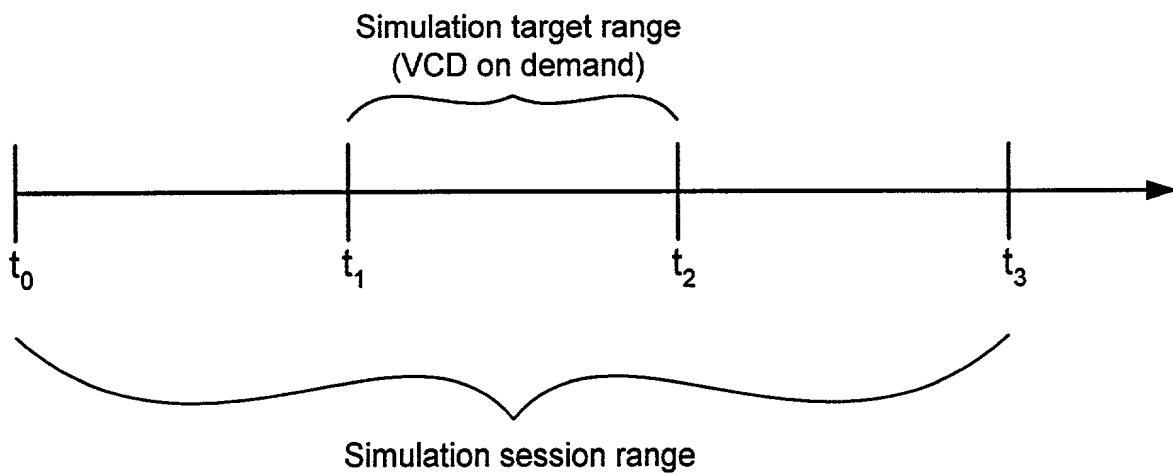


FIG. 84

SINGLE-ROW FPGA PER BOARD

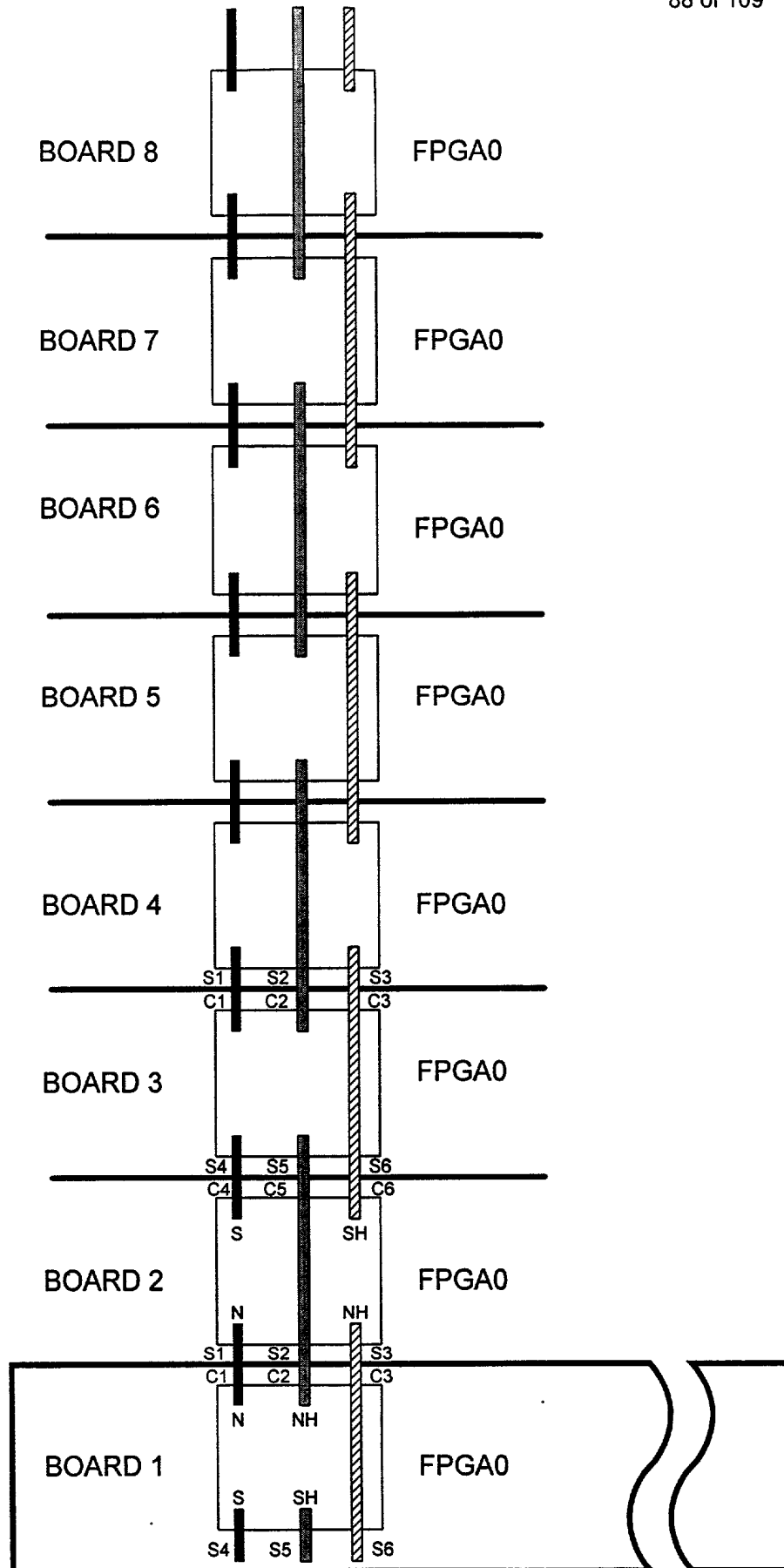


FIG. 85

TWO-ROW FPGA PER BOARD

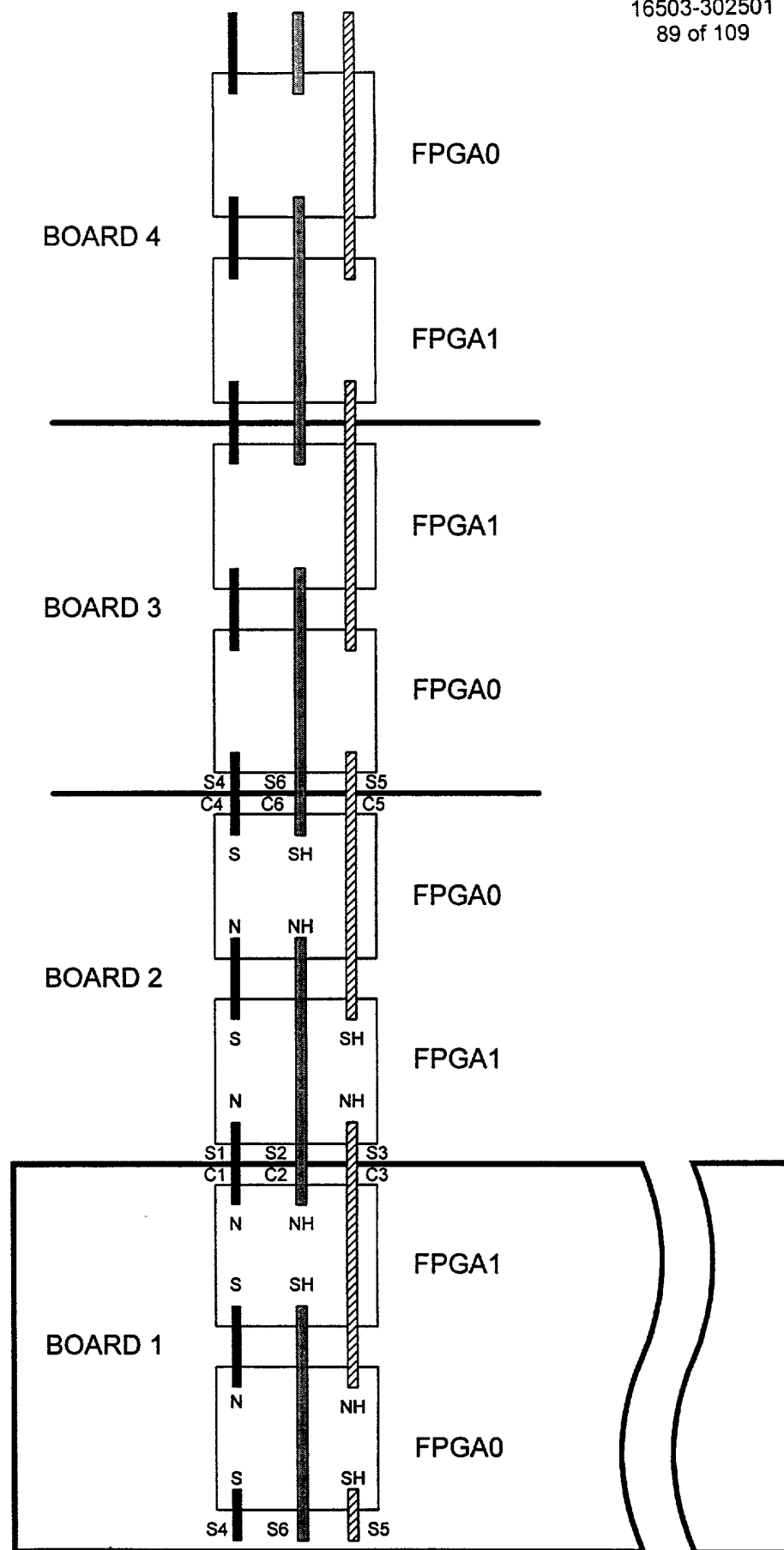


FIG. 86

THREE-ROW FPGA PER BOARD

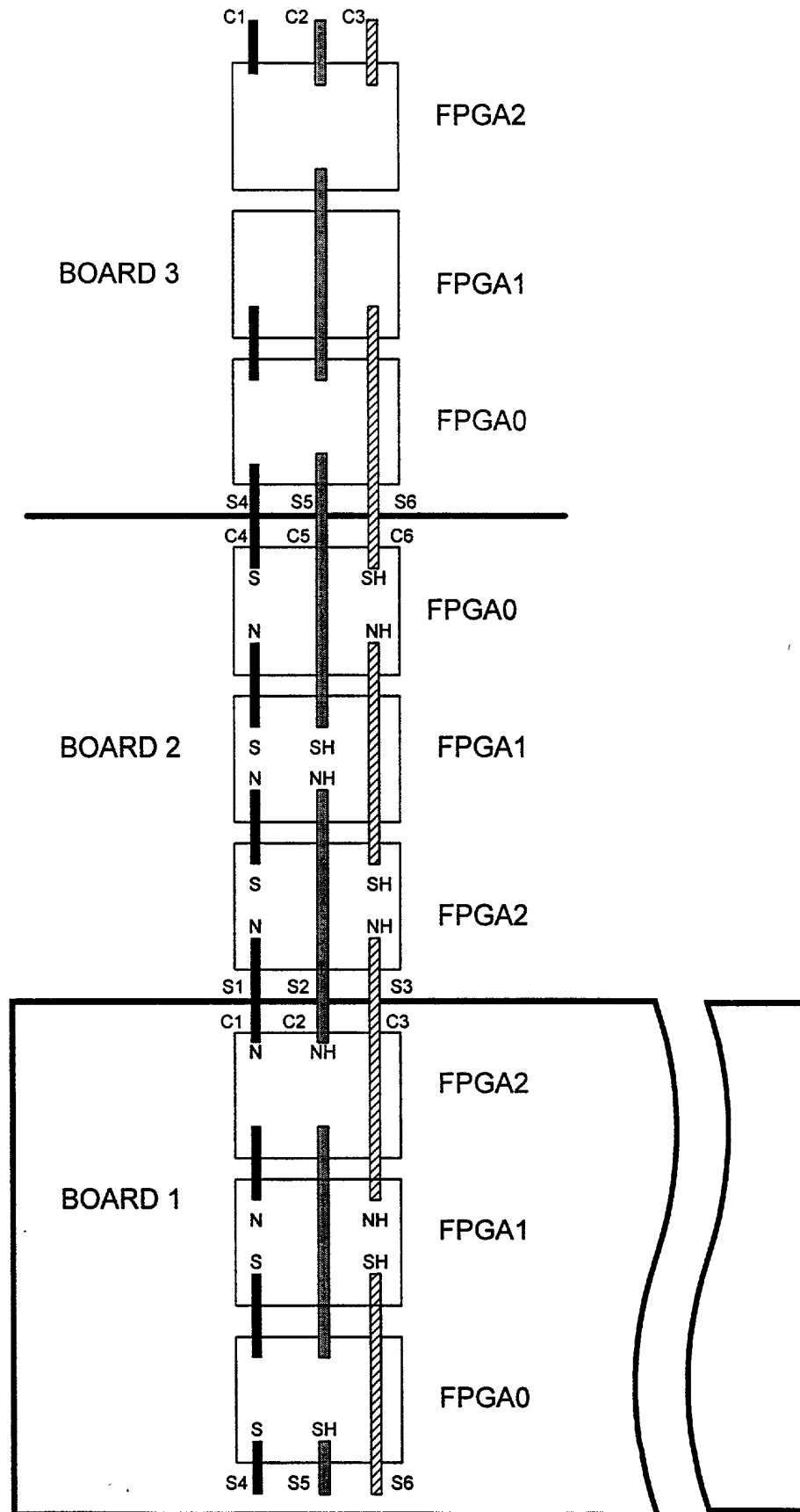


FIG. 87

FOUR-ROW FPGA PER BOARD

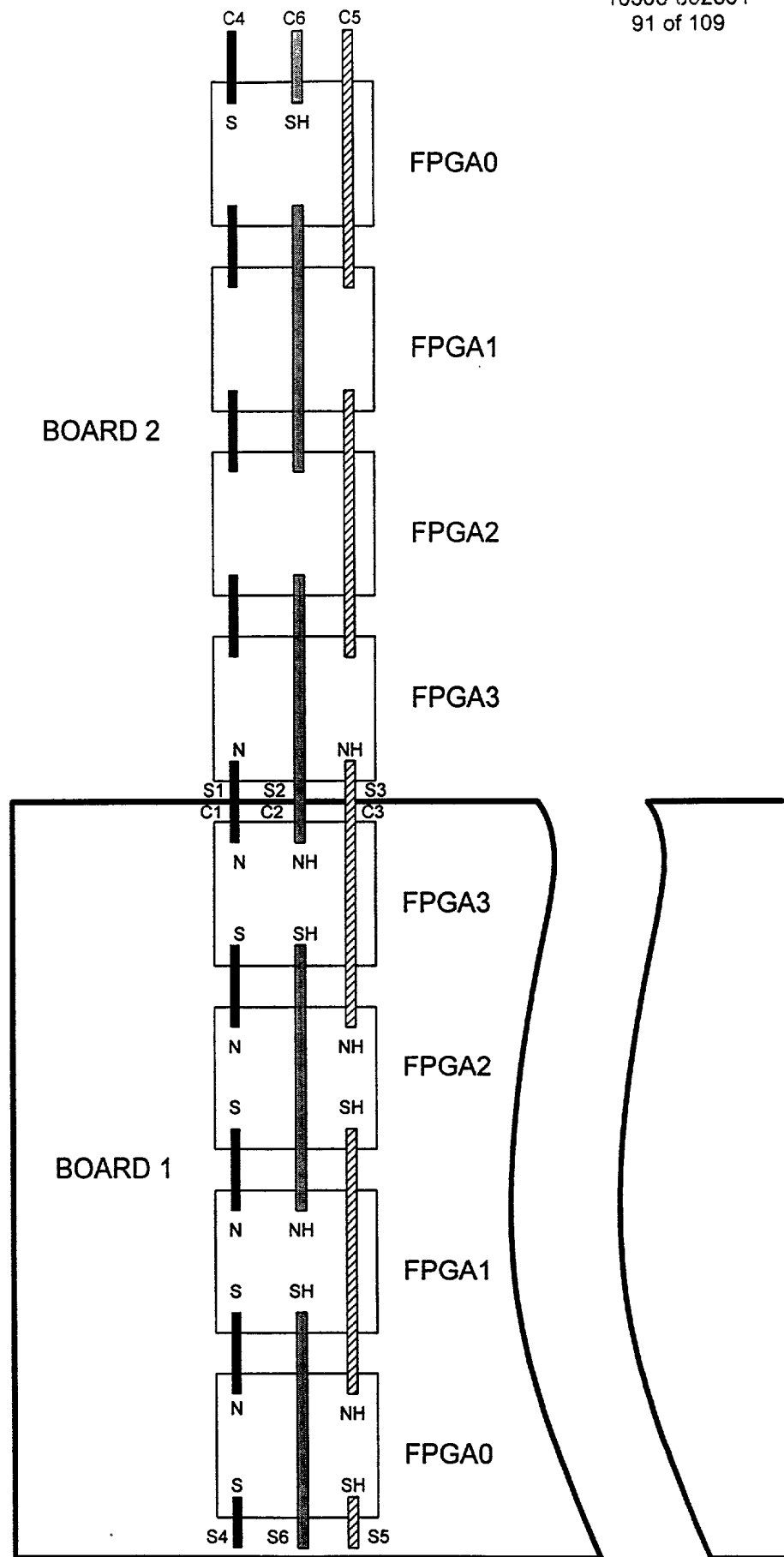


FIG. 88

INTERCONNECT FOR THREE-ROW PER BOARD

I/O Signals	Odd Board	Even Board	Common Board
	Connector-Group Pin-position	Connector-Group Pin-position	Connector-Group Pin-position
FPGA2_N	C1	S1	C1, S1
FPGA2_NH	C2	S3	C2, S3
FPGA1_NH	C3	S2	C3, S2
FPGA0_S	S4	C4	C4, S4
FPGA0_SH	S5	C6	C6, S5
FPGA1_SH	S6	C5	C5, S6

FIG. 89

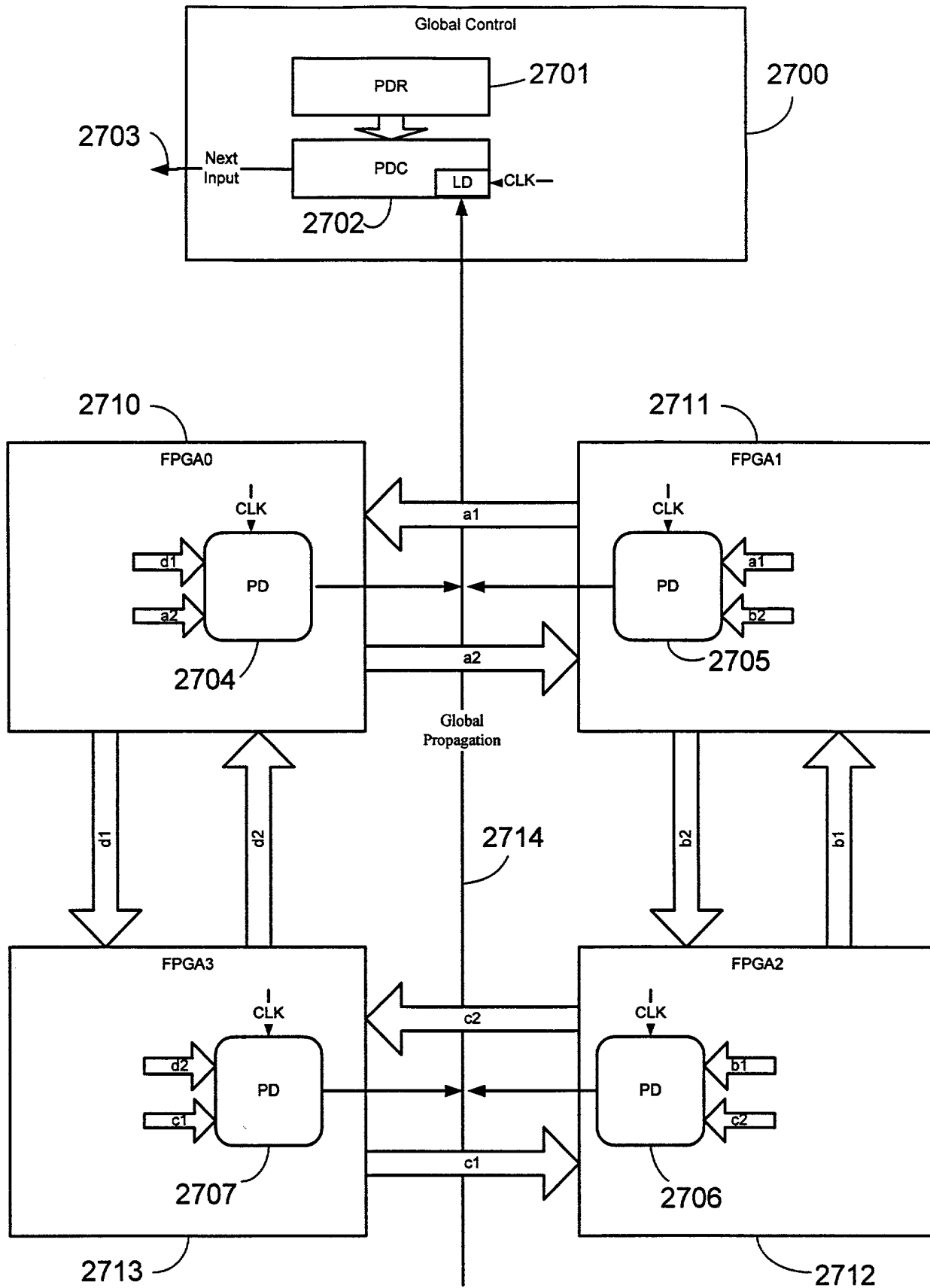


FIG. 90

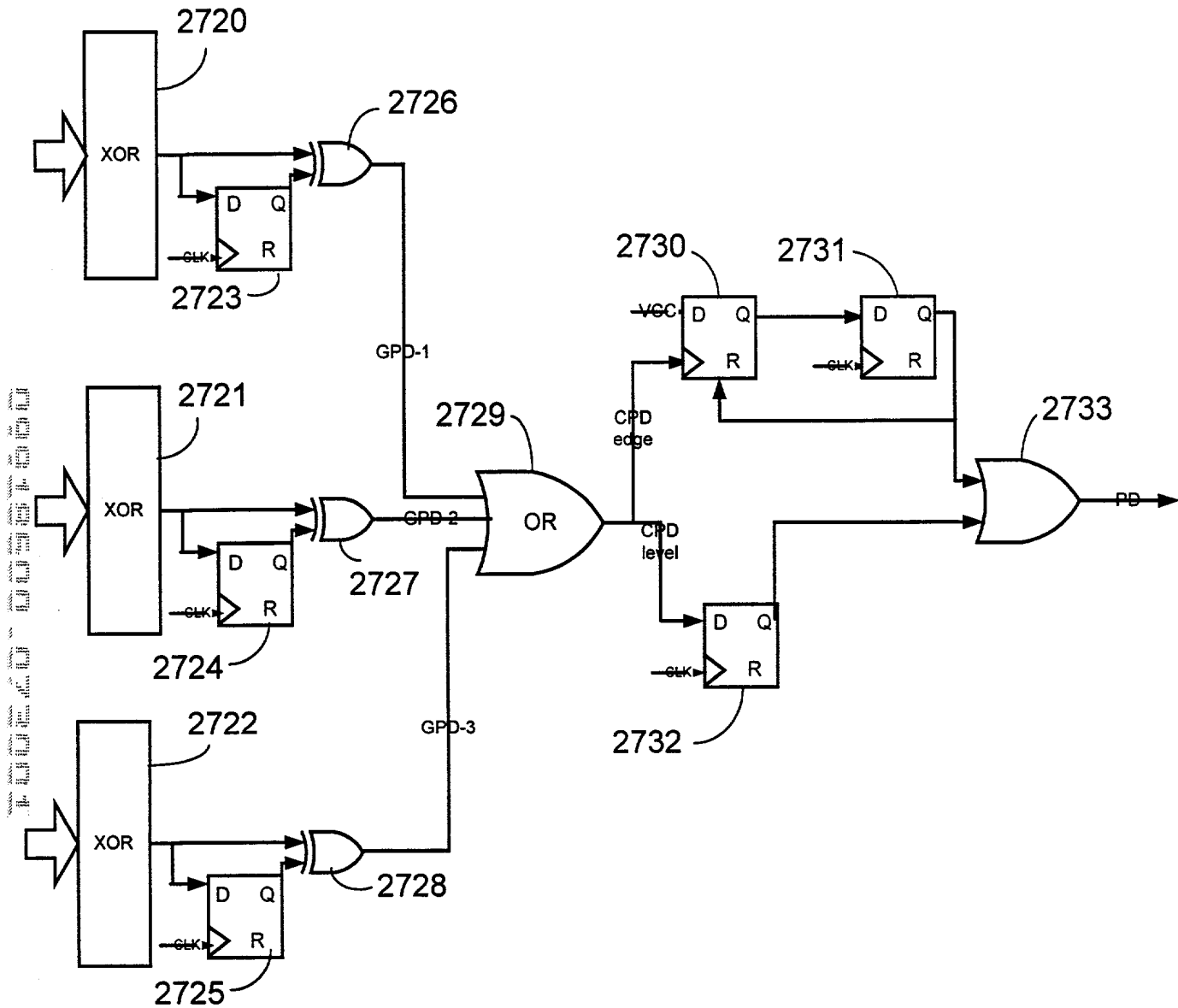


FIG. 91

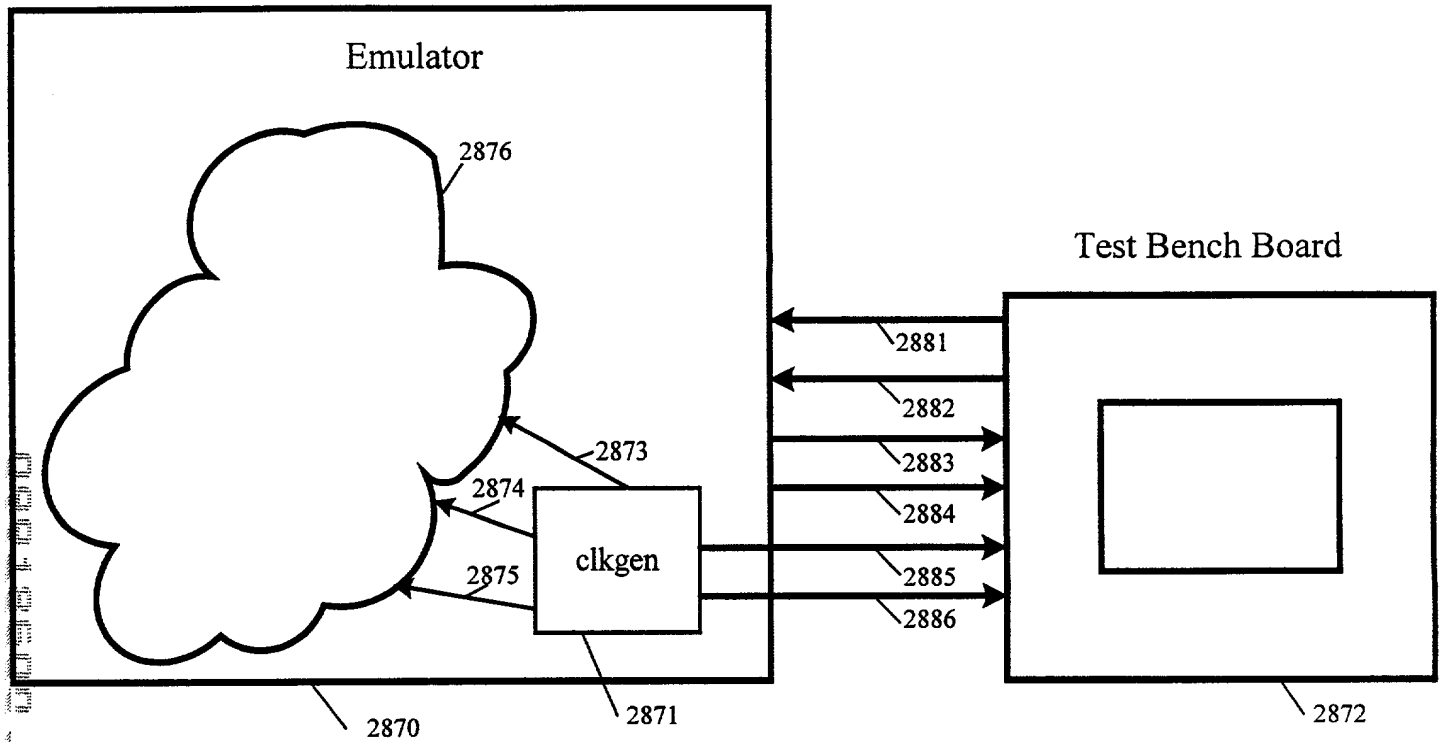


FIG. 92

Clock Specification

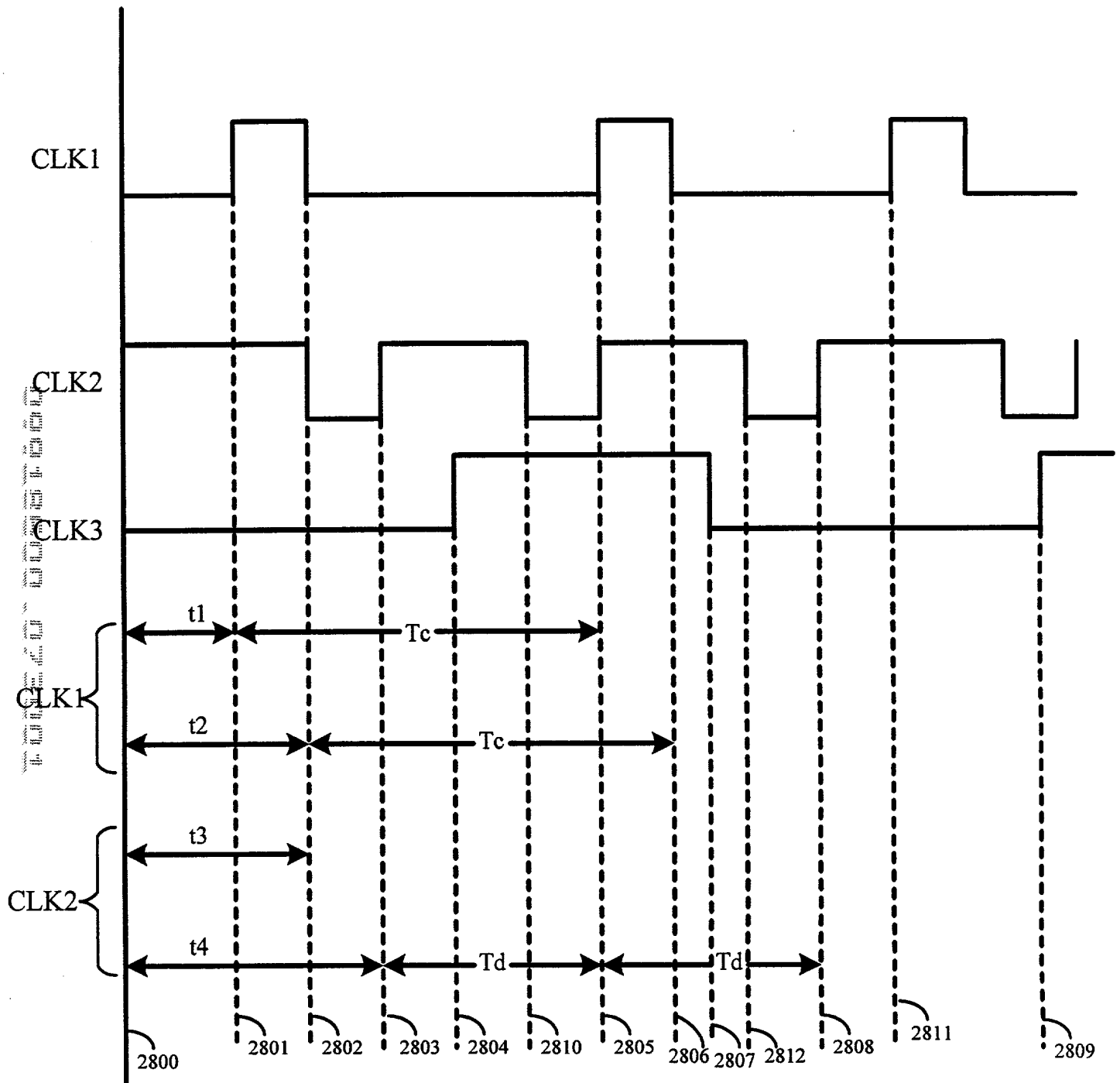


FIG. 93

Clock Generation Scheduler w/ Slices

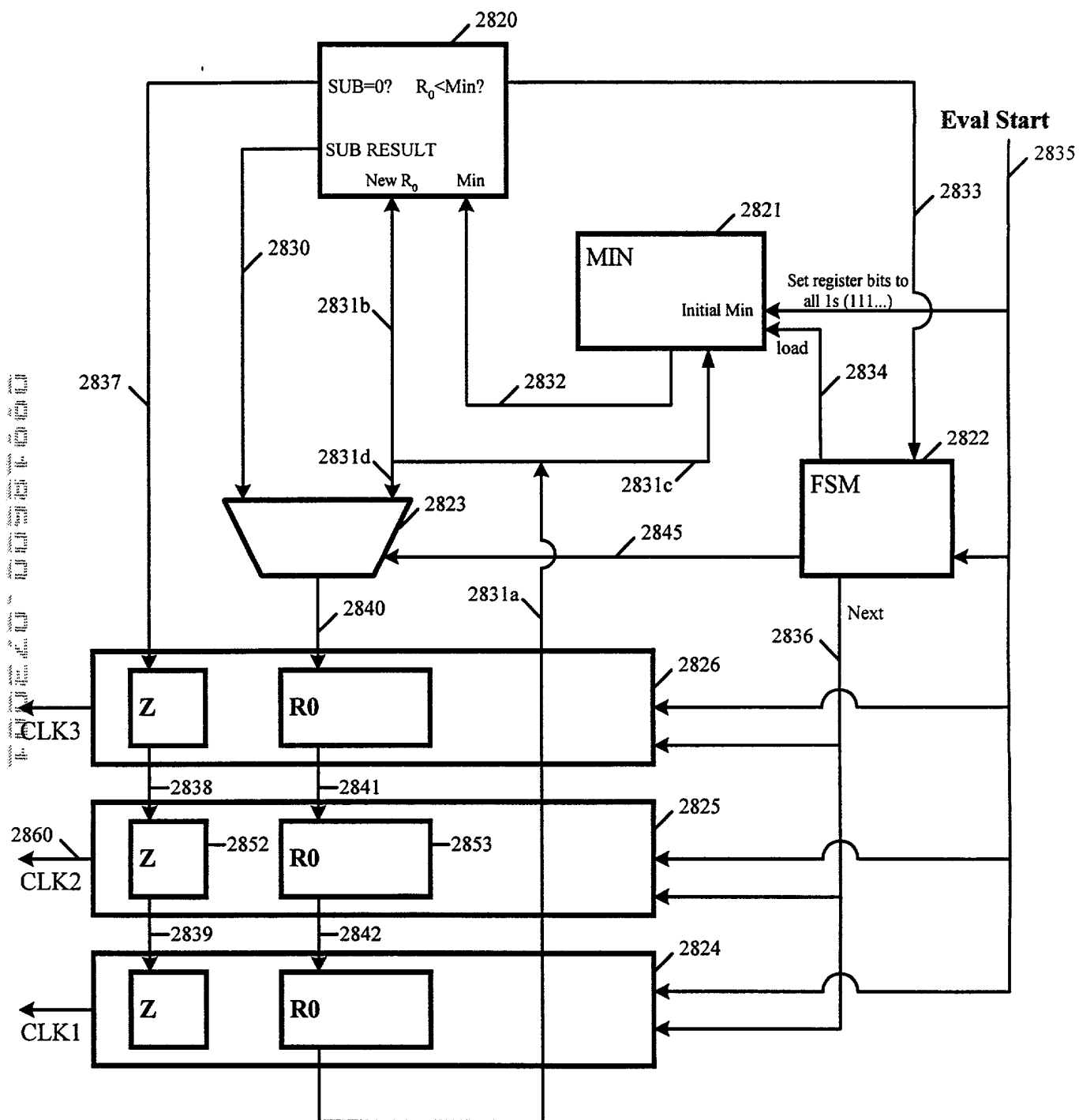


FIG. 94

Clock Generation Slice

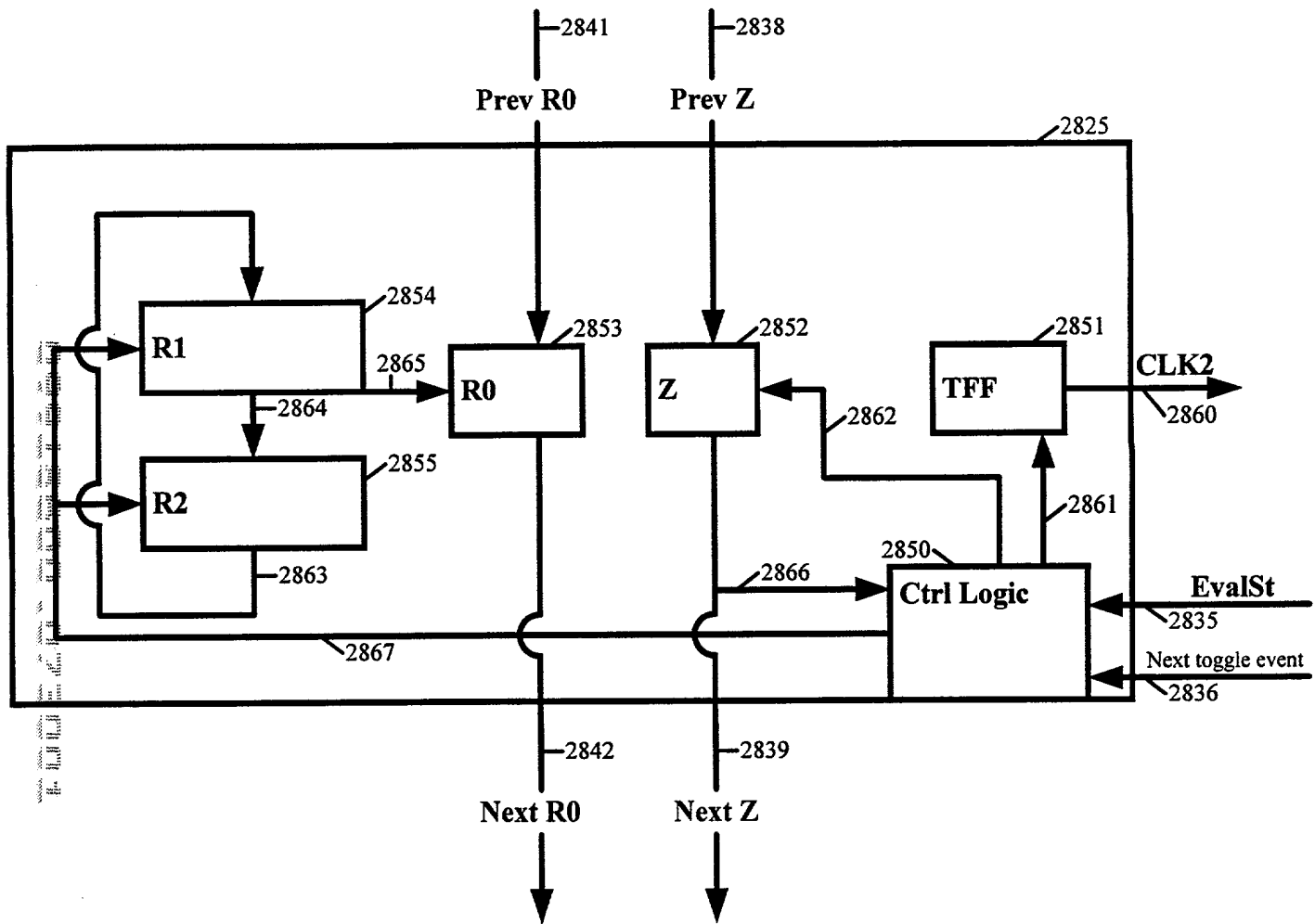


FIG. 95

Clock Generation Scheduler and Slices

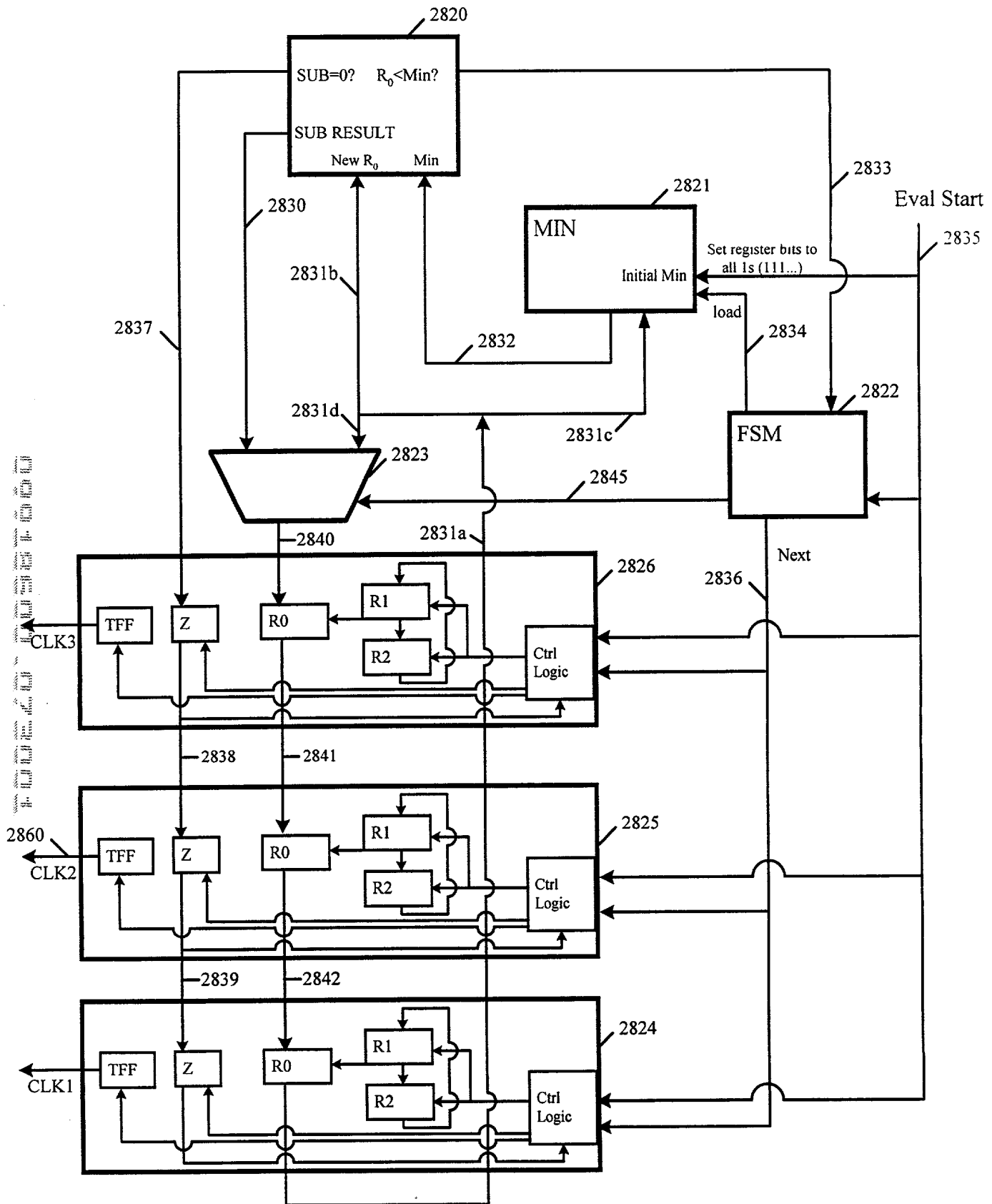


FIG. 96



FIG. 97

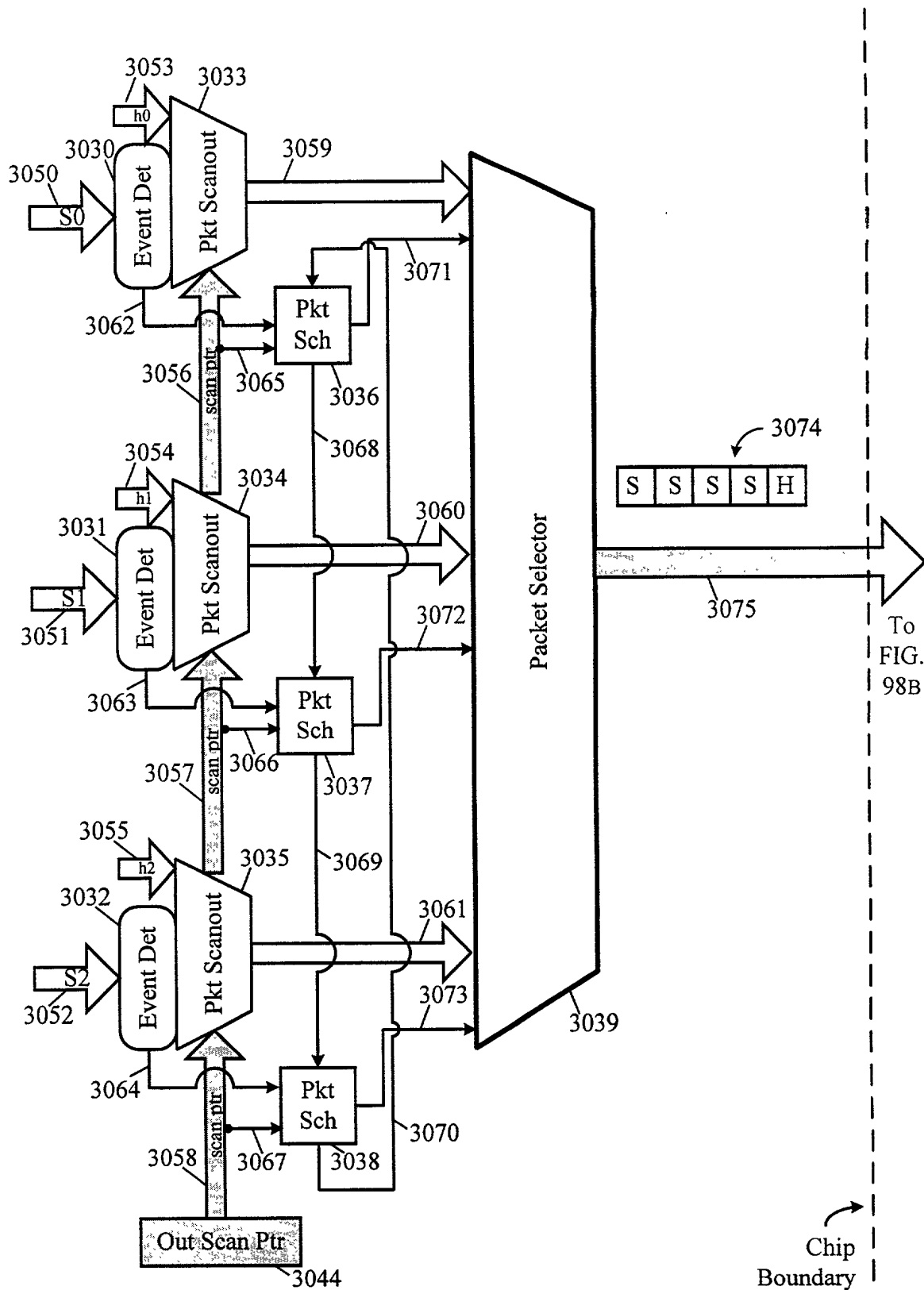


FIG. 98A

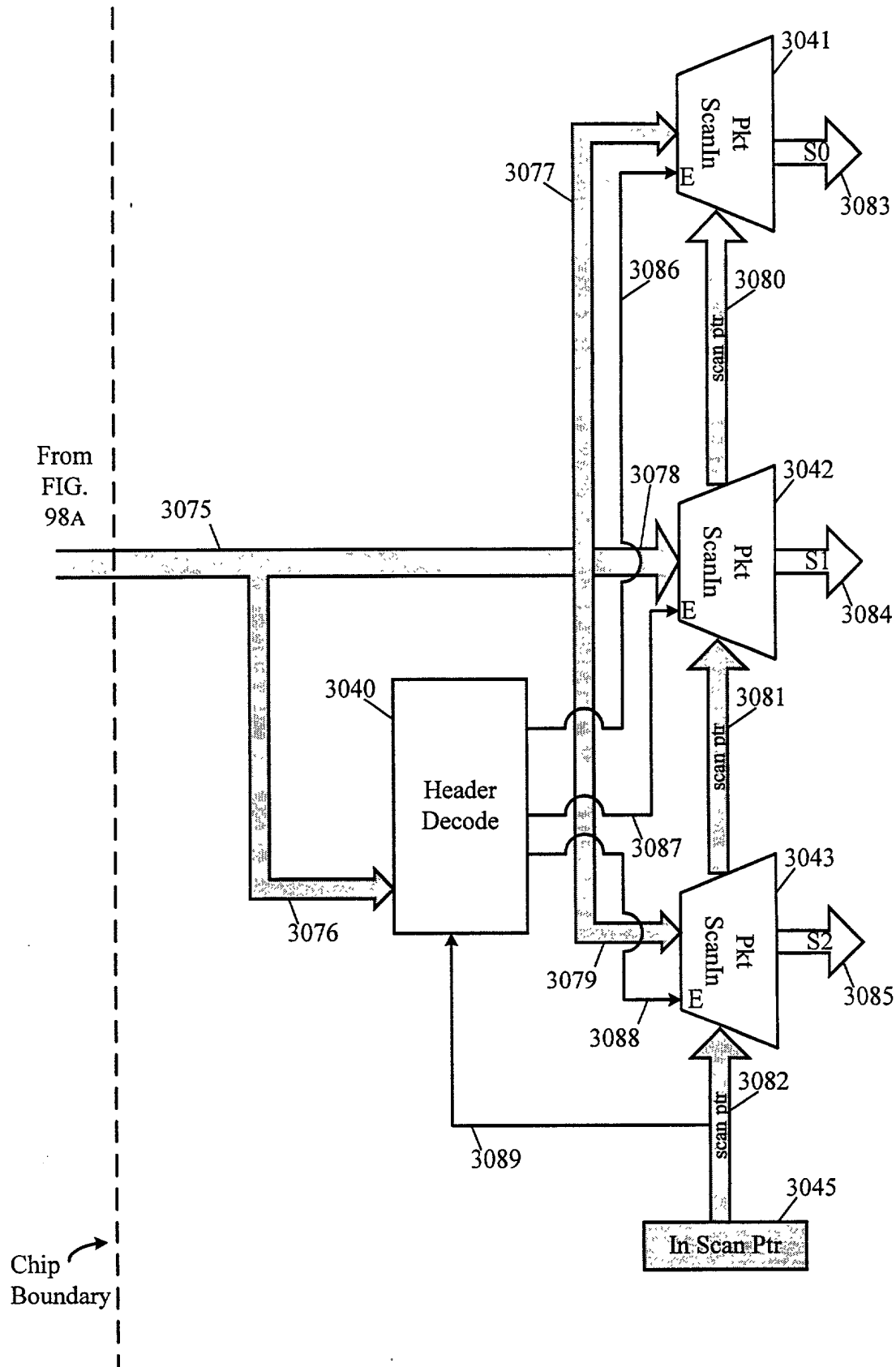


FIG. 98B

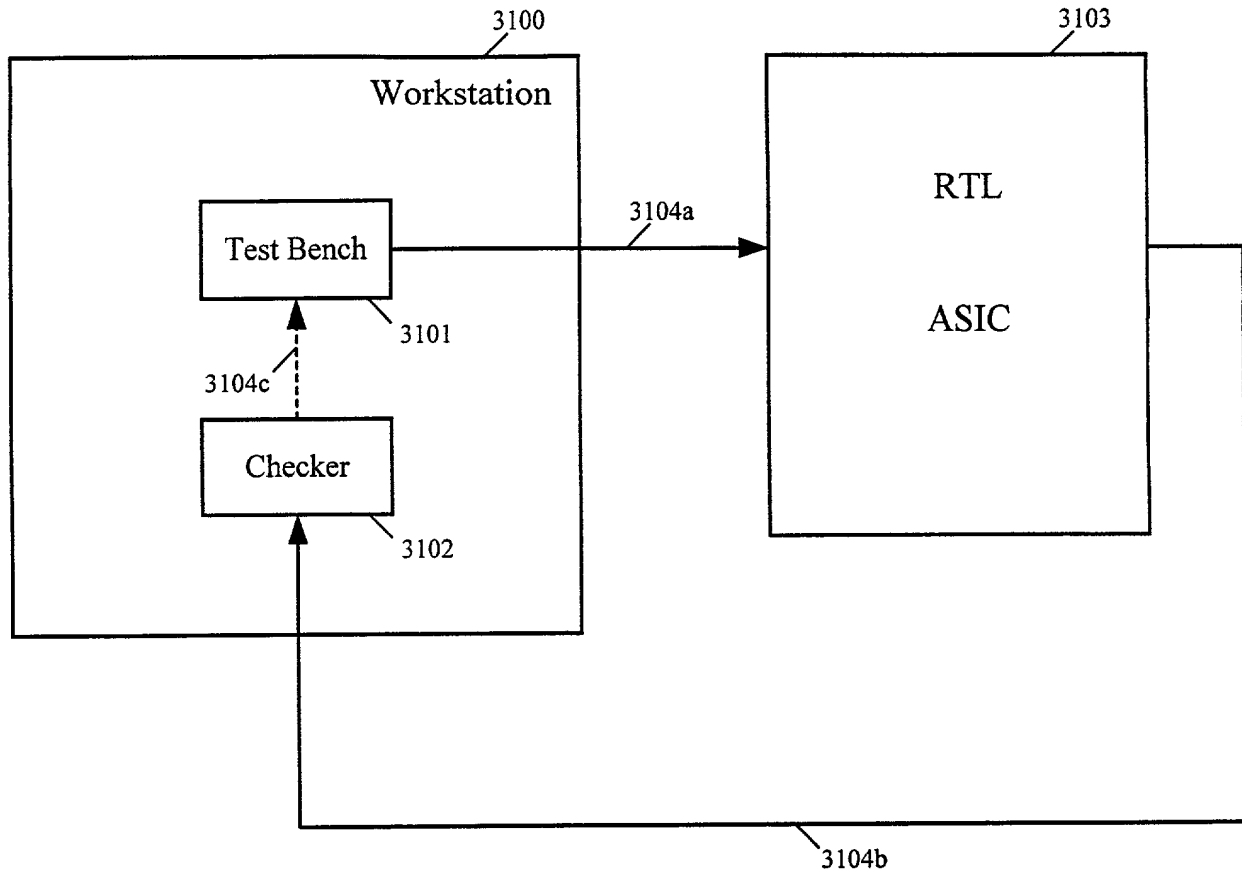


FIG. 99

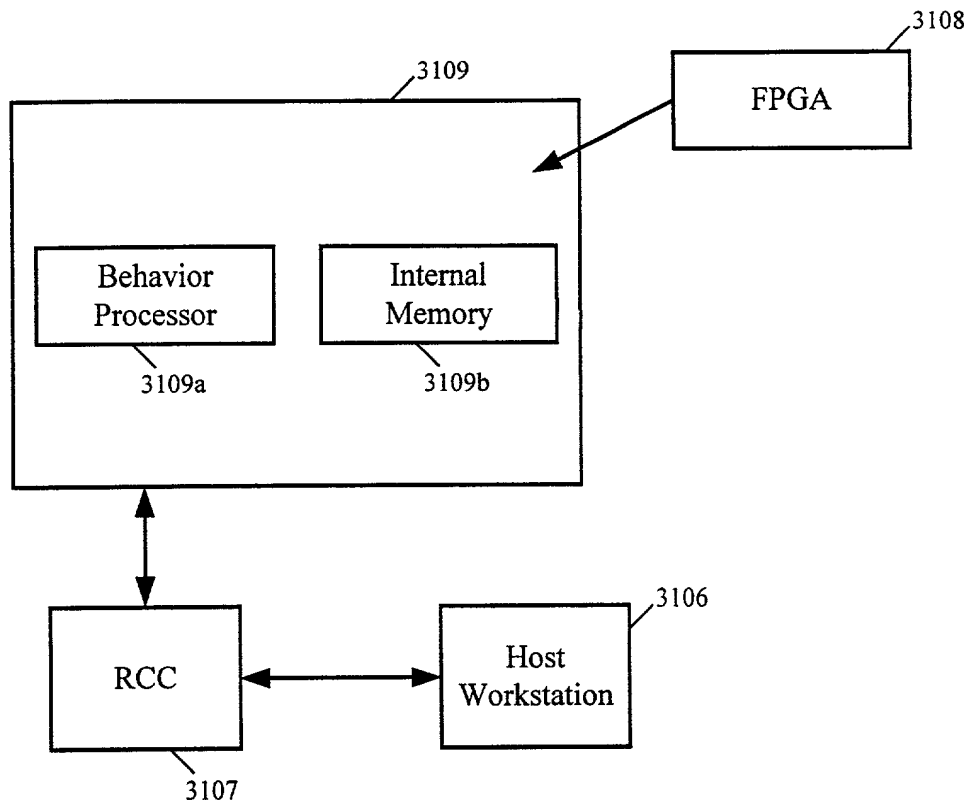


FIG. 100

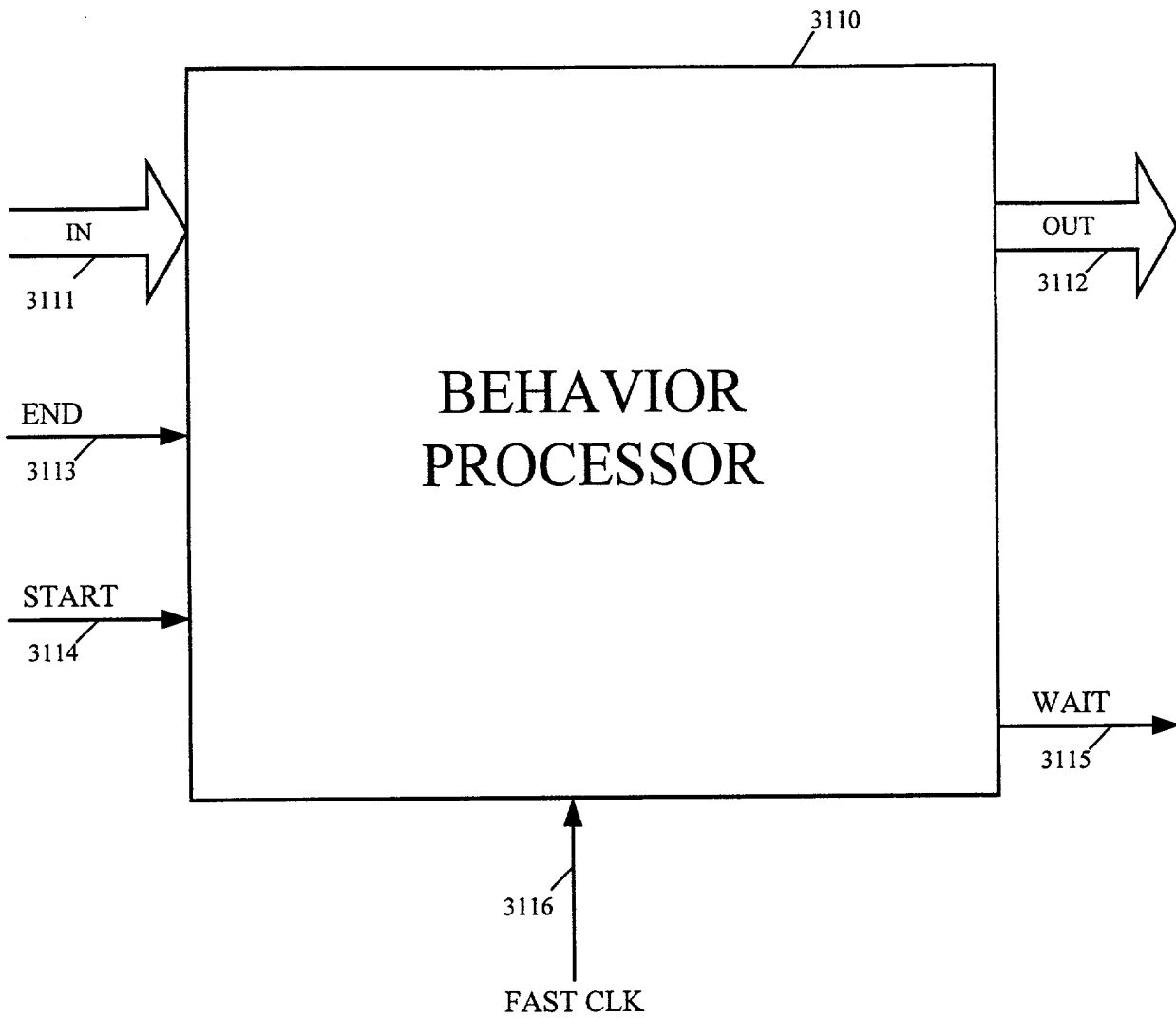


FIG. 101

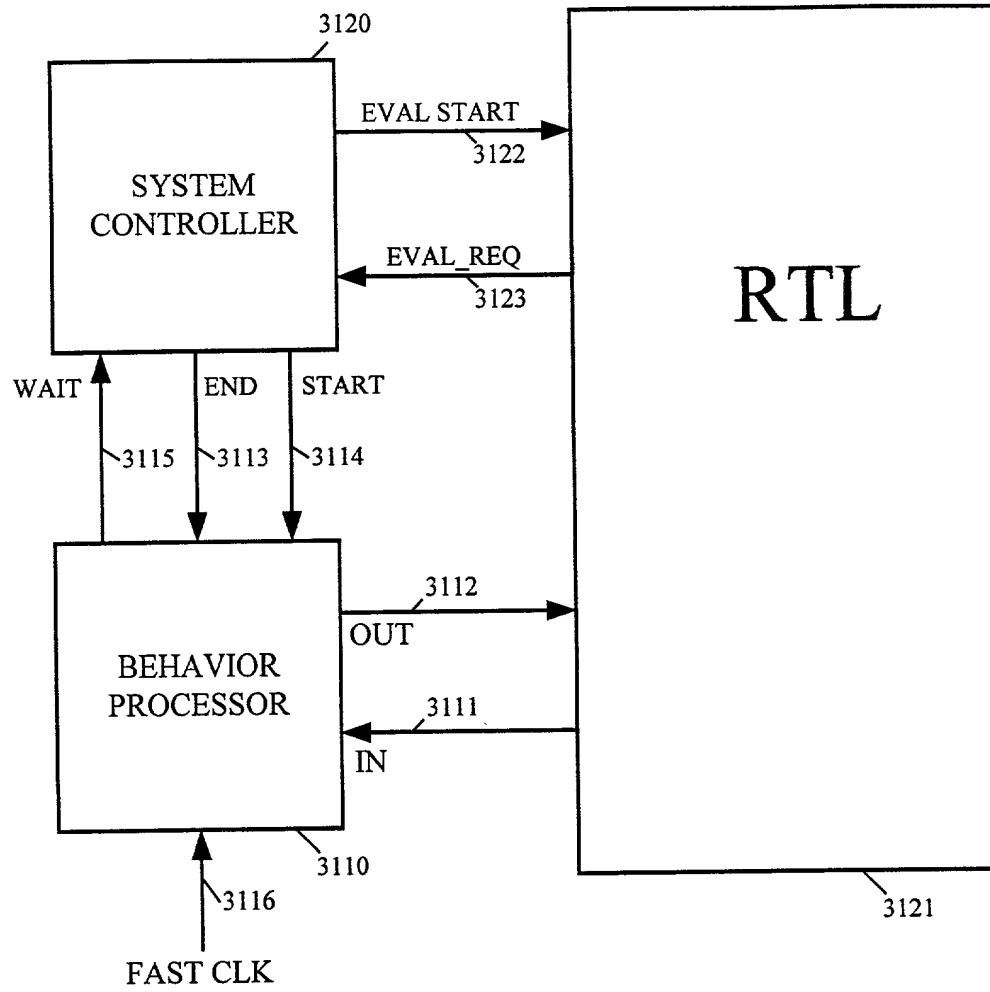


FIG. 102

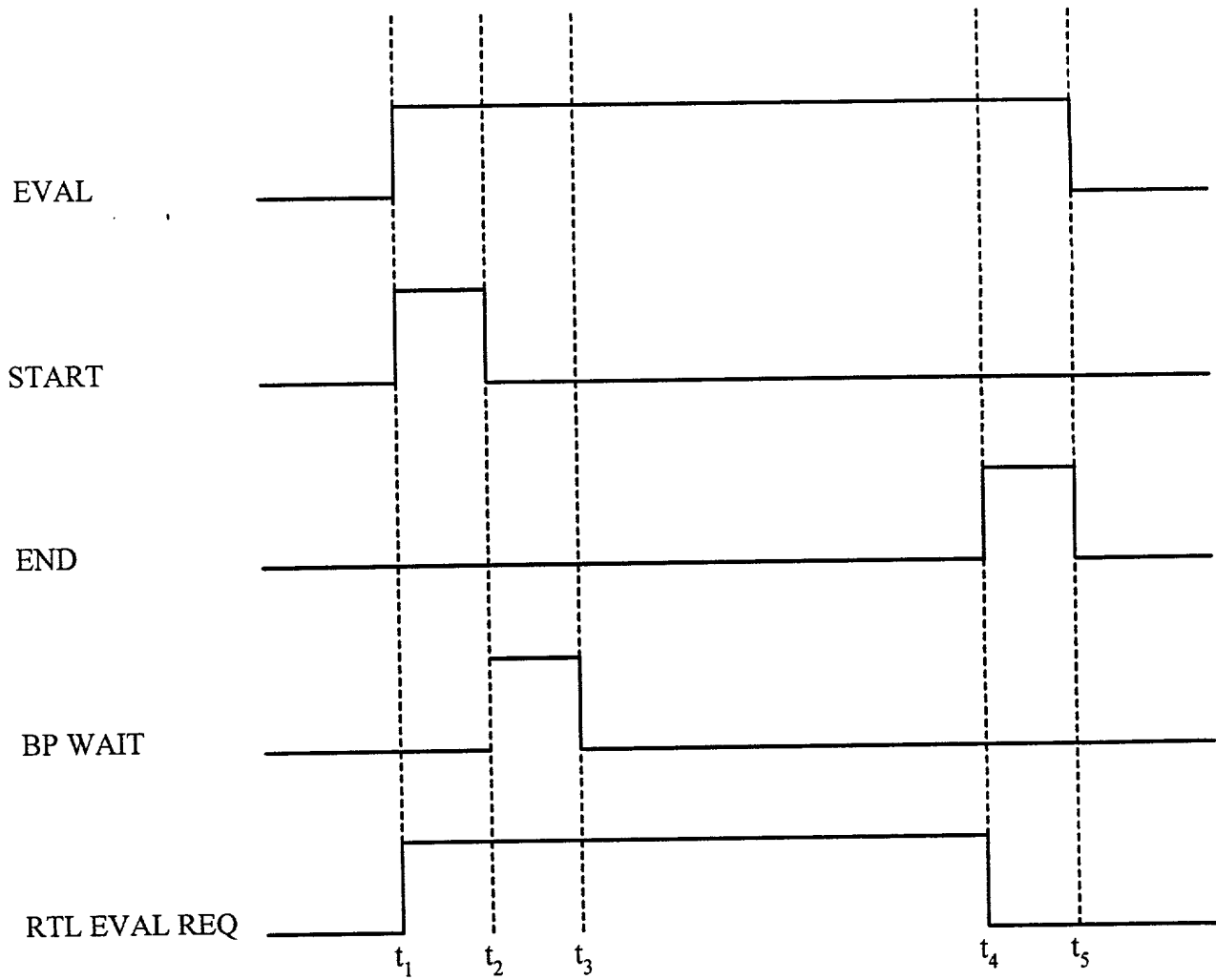


FIG. 103

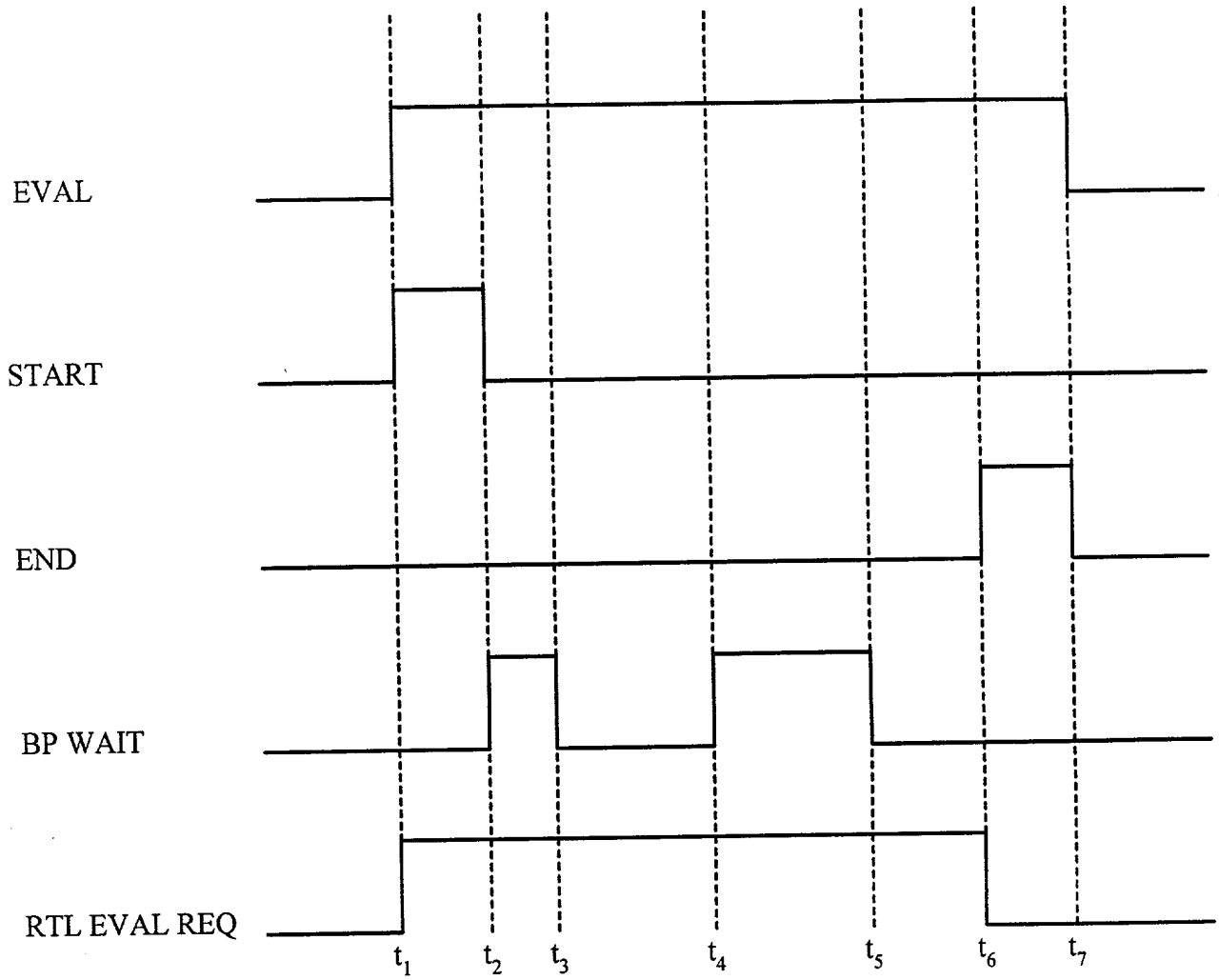


FIG. 104

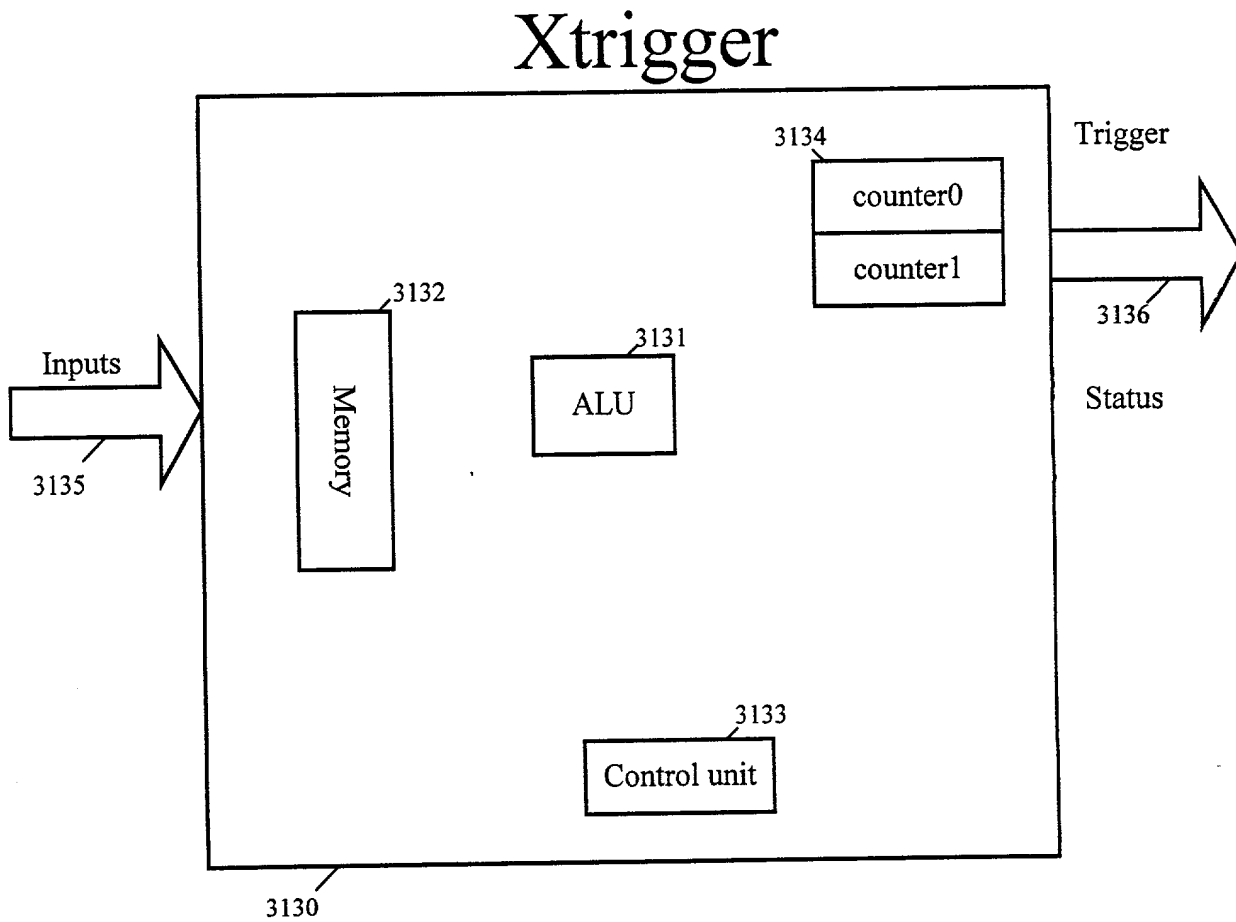


FIG. 105